//TEAM NOR COMPLETE NETLIST!!!

simulator lang=spectre

parameters r=1.25

//TOTAL WIDTH = 15899.25um

//WCD = 8.059nsec

//ENERGY per CYCLE = 702.867pJ

//THE METRIC: 7.2579E-25 sec^2\*m\*J

//====================================================

// Library Links

//====================================================

include "/net/cadence/ncsu-cdk/ncsu-cdk-1.5.1/models/spectre/standalone/ami06P.m"

include "/net/cadence/ncsu-cdk/ncsu-cdk-1.5.1/models/spectre/standalone/ami06N.m"

//====================================================

// Sources - power supplies and inputs

//====================================================

Vmain (vdd! 0) vsource type=dc dc=pvdd

//====================================================

// Netlist

//====================================================

/////////////////

//SIMPLE STUFF://

/////////////////

// Library name: Tutorial

// Cell name: bcInverter

// View name: schematic

// width = 3.375um

subckt bcInverter Vdd Vss in out

parameters wp=r\*1.5u wn=1.5u ln=600n lp=600n mult=1

P0 (out in Vdd Vdd) ami06P w=wp l=lp as=1.5u\*wp ad=1.5u\*wp ps=3u+wp \

pd=3u+wp m=mult region=sat

N0 (out in Vss Vss) ami06N w=wn l=ln as=1.5u\*wn ad=1.5u\*wn ps=3u+wn \

pd=3u+wn m=mult region=sat

ends bcInverter

// End of subcircuit definition.

// Library name: Project

// Cell name: Tgate

// passbar must be opposite of pass

// width = 3.375um

subckt Tgate Vdd Vss in out pass passbar

parameters wp=r\*1.5u wn=1.5u ln=600n lp=600n mult=1

P0 (out passbar in Vdd) ami06P w=wp l=lp as=1.5u\*wp ad=1.5u\*wp ps=3u+wp \

pd=3u+wp m=mult region=sat

N0 (in pass out Vss) ami06N w=wn l=ln as=1.5u\*wn ad=1.5u\*wn ps=3u+wn \

pd=3u+wn m=mult region=sat

ends Tgate

// End of subcircuit definition.

////////////

//SHIFTER://

////////////////////////////////////////////////////////////////////////////////////////////////

//1 bit Shifter

//width = 13.5um

subckt Shifter1b Vdd Vss in Sel0 Sel1 Sel2 Sel3 Sel0b Sel1b Sel2b Sel3b Sh1 Sh2 Sh3 Sh4

I0 (Vdd Vss in Sh1 Sel0 Sel0b) Tgate

//wp=1.5u

I1 (Vdd Vss in Sh2 Sel1 Sel1b) Tgate

//wp=1.5u

I2 (Vdd Vss in Sh3 Sel2 Sel2b) Tgate

//wp=1.5u

I3 (Vdd Vss in Sh4 Sel3 Sel3b) Tgate

//wp=1.5u

ends Shifter1b

//4 output Decoder

// width = 62.25um

subckt Decoder4out Vdd Vss in0 in1 out0 out1 out2 out3 out0b out1b out2b out3b

parameters SInv=1 SNOR3=1 SNOR02=1

Inv0 (Vdd Vss in0 in0b) bcInverter

//wp=1.5u

Inv1 (Vdd Vss in1 in1b) bcInverter

//wp=1.5u

NOR0 (Vdd Vss in0 in1 out0) NOR2in //wp=2\*1.5u

NOR1 (Vdd Vss in0b in1 out1) NOR2in //wp=2\*1.5u

NOR2 (Vdd Vss in0 in1b out2) NOR2in //wp=2\*1.5u

NOR3 (Vdd Vss in0b in1b out3) NOR2in //wp=2\*1.5u

Invout0 (Vdd Vss out0 out0b) bcInverter //wp=1.5u

Invout1 (Vdd Vss out1 out1b) bcInverter

//wp=1.5u

Invout2 (Vdd Vss out2 out2b) bcInverter //wp=1.5u

Invout3 (Vdd Vss out3 out3b) bcInverter

//wp=1.5u

ends Decoder4out

//16 bit shifter

//width = 386.25

subckt Shifter16b Vdd Vss inA0 inA1 inA2 inA3 inA4 inA5 inA6 inA7 inA8 inA9\

inA10 inA11 inA12 inA13 inA14 inA15 inB0 inB1 Aout0 Aout1\

Aout2 Aout3 Aout4 Aout5 Aout6 Aout7 Aout8 Aout9 Aout10\

Aout11 Aout12 Aout13 Aout14 Aout15

IBuf0a (Vdd Vss outputA0 ShBuf0) bcInverter

//wp=1.5u

IBuf0b (Vdd Vss ShBuf0 Aout0) bcInverter

//wp=1.5u

IBuf1a (Vdd Vss outputA1 ShBuf1) bcInverter

//wp=1.5u

IBuf1b (Vdd Vss ShBuf1 Aout1) bcInverter //

wp=1.5u

IBuf2a (Vdd Vss outputA2 ShBuf2) bcInverter

//wp=1.5u

IBuf2b (Vdd Vss ShBuf2 Aout2) bcInverter //

wp=1.5u

IBuf3a (Vdd Vss outputA3 ShBuf3) bcInverter

//wp=1.5u

IBuf3b (Vdd Vss ShBuf3 Aout3) bcInverter //

wp=1.5u

IBuf4a (Vdd Vss outputA4 ShBuf4) bcInverter

//wp=1.5u

IBuf4b (Vdd Vss ShBuf4 Aout4) bcInverter //

wp=1.5u

IBuf5a (Vdd Vss outputA5 ShBuf5) bcInverter

//wp=1.5u

IBuf5b (Vdd Vss ShBuf5 Aout5) bcInverter //wp=1.5u

IBuf6a (Vdd Vss outputA6 ShBuf6) bcInverter

//wp=1.5u

IBuf6b (Vdd Vss ShBuf6 Aout6) bcInverter

//wp=1.5u

IBuf7a (Vdd Vss outputA7 ShBuf7) bcInverter

//wp=1.5u

IBuf7b (Vdd Vss ShBuf7 Aout7) bcInverter

//wp=1.5u

IBuf8a (Vdd Vss outputA8 ShBuf8) bcInverter

//wp=1.5u

IBuf8b (Vdd Vss ShBuf8 Aout8) bcInverter //

wp=1.5u

IBuf9a (Vdd Vss outputA9 ShBuf9) bcInverter

//wp=1.5u

IBuf9b (Vdd Vss ShBuf9 Aout9) bcInverter //

wp=1.5u

IBuf10a (Vdd Vss outputA10 ShBuf10) bcInverter

//wp=1.5u

IBuf10b (Vdd Vss ShBuf10 Aout10) bcInverter //

wp=1.5u

IBuf11a (Vdd Vss outputA11 ShBuf11) bcInverter

//wp=1.5u

IBuf11b (Vdd Vss ShBuf11 Aout11) bcInverter //

wp=1.5u

IBuf12a (Vdd Vss outputA12 ShBuf12) bcInverter

//wp=1.5u

IBuf12b (Vdd Vss ShBuf12 Aout12) bcInverter //

wp=1.5u

IBuf13a (Vdd Vss outputA13 ShBuf13) bcInverter

//wp=1.5u

IBuf13b (Vdd Vss ShBuf13 Aout13) bcInverter //

wp=1.5u

IBuf14a (Vdd Vss outputA14 ShBuf14) bcInverter

//wp=1.5u

IBuf14b (Vdd Vss ShBuf14 Aout14) bcInverter

//wp=1.5u

IBuf15a (Vdd Vss outputA15 ShBuf15) bcInverter

//wp=1.5u

IBuf15b (Vdd Vss ShBuf15 Aout15) bcInverter

//wp=1.5u

Decoder (Vdd Vss inB0 inB1 Sh1 Sh2 Sh3 Sh4 Sh1b Sh2b Sh3b Sh4b) Decoder4out

Tgatem4 (Vdd Vss Vss outputA0 Sh4 Sh4b) Tgate

//wp=1.5u

Tgatem3a (Vdd Vss Vss outputA0 Sh3 Sh3b) Tgate

//wp=1.5u

Tgatem3b (Vdd Vss Vss outputA1 Sh4 Sh4b) Tgate

//wp=1.5u

Tgatem2a (Vdd Vss Vss outputA0 Sh2 Sh2b) Tgate

//wp=1.5u

Tgatem2b (Vdd Vss Vss outputA1 Sh3 Sh3b) Tgate

//wp=1.5u

Tgatem2c (Vdd Vss Vss outputA2 Sh4 Sh4b) Tgate

//wp=1.5u

Shifterm1 (Vdd Vss Vss Sh1 Sh2 Sh3 Sh4 Sh1b Sh2b Sh3b Sh4b outputA0 outputA1 outputA2 outputA3) Shifter1b

Shifter0 (Vdd Vss inA0 Sh1 Sh2 Sh3 Sh4 Sh1b Sh2b Sh3b Sh4b outputA1 outputA2 outputA3 outputA4) Shifter1b

Shifter1 (Vdd Vss inA1 Sh1 Sh2 Sh3 Sh4 Sh1b Sh2b Sh3b Sh4b outputA2 outputA3 outputA4 outputA5) Shifter1b

Shifter2 (Vdd Vss inA2 Sh1 Sh2 Sh3 Sh4 Sh1b Sh2b Sh3b Sh4b outputA3 outputA4 outputA5 outputA6) Shifter1b

Shifter3 (Vdd Vss inA3 Sh1 Sh2 Sh3 Sh4 Sh1b Sh2b Sh3b Sh4b outputA4 outputA5 outputA6 outputA7) Shifter1b

Shifter4 (Vdd Vss inA4 Sh1 Sh2 Sh3 Sh4 Sh1b Sh2b Sh3b Sh4b outputA5 outputA6 outputA7 outputA8) Shifter1b

Shifter5 (Vdd Vss inA5 Sh1 Sh2 Sh3 Sh4 Sh1b Sh2b Sh3b Sh4b outputA6 outputA7 outputA8 outputA9) Shifter1b

Shifter6 (Vdd Vss inA6 Sh1 Sh2 Sh3 Sh4 Sh1b Sh2b Sh3b Sh4b outputA7 outputA8 outputA9 outputA10) Shifter1b

Shifter7 (Vdd Vss inA7 Sh1 Sh2 Sh3 Sh4 Sh1b Sh2b Sh3b Sh4b outputA8 outputA9 outputA10 outputA11) Shifter1b

Shifter8 (Vdd Vss inA8 Sh1 Sh2 Sh3 Sh4 Sh1b Sh2b Sh3b Sh4b outputA9 outputA10 outputA11 outputA12) Shifter1b

Shifter9 (Vdd Vss inA9 Sh1 Sh2 Sh3 Sh4 Sh1b Sh2b Sh3b Sh4b outputA10 outputA11 outputA12 outputA13) Shifter1b

Shifter10 (Vdd Vss inA10 Sh1 Sh2 Sh3 Sh4 Sh1b Sh2b Sh3b Sh4b outputA11 outputA12 outputA13 outputA14) Shifter1b

Shifter11 (Vdd Vss inA11 Sh1 Sh2 Sh3 Sh4 Sh1b Sh2b Sh3b Sh4b outputA12 outputA13 outputA14 outputA15) Shifter1b

Tgate12a (Vdd Vss inA12 outputA13 Sh1 Sh1b) Tgate

//wp=1.5u

Tgate12b (Vdd Vss inA12 outputA14 Sh2 Sh2b) Tgate

//wp=1.5u

Tgate12c (Vdd Vss inA12 outputA15 Sh3 Sh3b) Tgate

//wp=1.5u

Tgate13a (Vdd Vss inA13 outputA14 Sh1 Sh1b) Tgate

//wp=1.5u

Tgate13b (Vdd Vss inA13 outputA15 Sh2 Sh2b) Tgate

//wp=1.5u

Tgate14 (Vdd Vss inA14 outputA15 Sh1 Sh1b) Tgate

//wp=1.5u

ends Shifter16b

//////////////////////

//MUXes AND DEMUXes://

//////////////////////////////////////////////////////////////////////////////////////////////////////////

// Library name: Project

// Cell name: 2:1MUXBar

// View name: schematic

//width = 24.375um

subckt MUX21Bar Gnd Vdd in0 in1 inS out

parameters wp=2\*r\*1.5u wn=2\*1.5u ln=600n lp=600n mult=1

I0 (Vdd Gnd inS inSB) bcInverter

MPS (out inS midP Vdd) ami06P w=wp l=lp as=1.5u\*wp ad=1.5u\*wp ps=3u+wp \

pd=3u+wp m=mult region=sat

MPSn (midP inSB Vdd Vdd) ami06P w=wp l=lp as=1.5u\*wp ad=1.5u\*wp ps=3u+wp \

pd=3u+wp m=mult region=sat

MPB (out in1 midP Vdd) ami06P w=wp l=lp as=1.5u\*wp ad=1.5u\*wp ps=3u+wp \

pd=3u+wp m=mult region=sat

MPA (midP in0 Vdd Vdd) ami06P w=wp l=lp as=1.5u\*wp ad=1.5u\*wp ps=3u+wp \

pd=3u+wp m=mult region=sat

MNSn (midNASbar inSB Gnd Gnd) ami06N w=wn l=ln as=1.5u\*wn ad=1.5u\*wn ps=3u+wn \

pd=3u+wn m=mult region=sat

MNS (midNBS inS Gnd Gnd) ami06N w=wn l=ln as=1.5u\*wn ad=1.5u\*wn ps=3u+wn \

pd=3u+wn m=mult region=sat

MNB (out in1 midNBS Gnd) ami06N w=wn l=ln as=1.5u\*wn ad=1.5u\*wn ps=3u+wn \

pd=3u+wn m=mult region=sat

MNA (out in0 midNASbar Gnd) ami06N w=wn l=ln as=1.5u\*wn ad=1.5u\*wn ps=3u+wn \

pd=3u+wn m=mult region=sat

ends MUX21Bar

// End of subcircuit definition.

// Library name: Project

// Cell name: 2:1MUX

// View name: schematic

//width = 27.75um

subckt MUX21 Gnd Vdd in0 in1 inS out

I1 (Vdd Gnd outBar out) bcInverter

MUX (Gnd Vdd in0 in1 inS outBar) MUX21Bar

ends MUX21

// End of subcircuit definition.

// Library name: Project

// Cell name: 8:1MUX

// View name: schematic

//width = 194.25um

subckt MUX81 Gnd Out Vdd in0 in1 in2 in3 in4 in5 in6 in7 inS0 inS1 inS2

I9 (Gnd Vdd in4 in5 inS0 net150) MUX21

I8 (Gnd Vdd in2 in3 inS0 net156) MUX21

I7 (Gnd Vdd in0 in1 inS0 net162) MUX21

I12 (Gnd Vdd net162 net156 inS1 net132) MUX21

I10 (Gnd Vdd in6 in7 inS0 net144) MUX21

I11 (Gnd Vdd net150 net144 inS1 net138) MUX21

I13 (Gnd Vdd net132 net138 inS2 Out) MUX21

ends MUX81

// End of subcircuit definition.

// Cell name: 16b2:1MUX

//width = 444um

subckt MUX16b21 VDD VSS A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10 A11 A12 A13 A14 A15 B0 B1 \

B2 B3 B4 B5 B6 B7 B8 B9 B10 B11 B12 B13 B14 B15 S Out0 Out1 Out2 Out3 \

Out4 Out5 Out6 Out7 Out8 Out9 Out10 Out11 Out12 Out13 Out14 Out15

I0 (VSS VDD A0 B0 S Out0) MUX21

I1 (VSS VDD A1 B1 S Out1) MUX21

I2 (VSS VDD A2 B2 S Out2) MUX21

I3 (VSS VDD A3 B3 S Out3) MUX21

I4 (VSS VDD A4 B4 S Out4) MUX21

I5 (VSS VDD A5 B5 S Out5) MUX21

I6 (VSS VDD A6 B6 S Out6) MUX21

I7 (VSS VDD A7 B7 S Out7) MUX21

I8 (VSS VDD A8 B8 S Out8) MUX21

I9 (VSS VDD A9 B9 S Out9) MUX21

I10 (VSS VDD A10 B10 S Out10) MUX21

I11 (VSS VDD A11 B11 S Out11) MUX21

I12 (VSS VDD A12 B12 S Out12) MUX21

I13 (VSS VDD A13 B13 S Out13) MUX21

I14 (VSS VDD A14 B14 S Out14) MUX21

I15 (VSS VDD A15 B15 S Out15) MUX21

ends MUX16b21

// Library name: Project

// Cell name: 16b8:1MUX

// View name: schematic

// width = 3108um

subckt MUX16b81 A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10 A11 A12 A13 A14 A15 B0 B1 \

B2 B3 B4 B5 B6 B7 B8 B9 B10 B11 B12 B13 B14 B15 C0 C1 C2 C3 C4 \

C5 C6 C7 C8 C9 C10 C11 C12 C13 C14 C15 D0 D1 D2 D3 D4 D5 D6 D7 \

D8 D9 D10 D11 D12 D13 D14 D15 E0 E1 E2 E3 E4 E5 E6 E7 E8 E9 E10 E11 \

E12 E13 E14 E15 F0 F1 F2 F3 F4 F5 F6 F7 F8 F9 F10 F11 F12 F13 F14 F15 \

G0 G1 G2 G3 G4 G5 G6 G7 G8 G9 G10 G11 G12 G13 G14 G15 H0 H1 H2 \

H3 H4 H5 H6 H7 H8 H9 H10 H11 H12 H13 H14 H15 Out0 Out1 Out2 Out3 \

Out4 Out5 Out6 Out7 Out8 Out9 Out10 Out11 Out12 Out13 Out14 Out15 S0 \

S1 S2 VDD VSS

I15 (VSS Out15 VDD A15 B15 C15 D15 E15 F15 G15 H15 S0 S1 S2) MUX81

I14 (VSS Out14 VDD A14 B14 C14 D14 E14 F14 G14 H14 S0 S1 S2) MUX81

I13 (VSS Out13 VDD A13 B13 C13 D13 E13 F13 G13 H13 S0 S1 S2) MUX81

I12 (VSS Out12 VDD A12 B12 C12 D12 E12 F12 G12 H12 S0 S1 S2) MUX81

I11 (VSS Out11 VDD A11 B11 C11 D11 E11 F11 G11 H11 S0 S1 S2) MUX81

I10 (VSS Out10 VDD A10 B10 C10 D10 E10 F10 G10 H10 S0 S1 S2) MUX81

I9 (VSS Out9 VDD A9 B9 C9 D9 E9 F9 G9 H9 S0 S1 S2) MUX81

I8 (VSS Out8 VDD A8 B8 C8 D8 E8 F8 G8 H8 S0 S1 S2) MUX81

I7 (VSS Out7 VDD A7 B7 C7 D7 E7 F7 G7 H7 S0 S1 S2) MUX81

I6 (VSS Out6 VDD A6 B6 C6 D6 E6 F6 G6 H6 S0 S1 S2) MUX81

I5 (VSS Out5 VDD A5 B5 C5 D5 E5 F5 G5 H5 S0 S1 S2) MUX81

I4 (VSS Out0 VDD A0 B0 C0 D0 E0 F0 G0 H0 S0 S1 S2) MUX81

I3 (VSS Out1 VDD A1 B1 C1 D1 E1 F1 G1 H1 S0 S1 S2) MUX81

I2 (VSS Out4 VDD A4 B4 C4 D4 E4 F4 G4 H4 S0 S1 S2) MUX81

I1 (VSS Out3 VDD A3 B3 C3 D3 E3 F3 G3 H3 S0 S1 S2) MUX81

I0 (VSS Out2 VDD A2 B2 C2 D2 E2 F2 G2 H2 S0 S1 S2) MUX81

ends MUX16b81

//1:6 DEMUX for A

//This DeMUX has following pass signals (S2,S1,S0):

// out0=(0,0,1)

// out1=(0,1,X)

// out2=(1,0,0)

// out3=(1,0,1)

// out4=(1,1,0)

// out5=(1,1,1)

//width = 219.375

subckt deMUX16 (Vdd Vss in S0 S1 S2 out0 out1 out2 out3 out4 out5)

NOR0 (Vdd Vss inB SBar0 S1 S2 out0) NOR4in

NOR1 (Vdd Vss inB SBar1 S2 out1) NOR3in

NOR2 (Vdd Vss inB S0 S1 SBar2 out2) NOR4in

NOR3 (Vdd Vss inB SBar0 S1 SBar2 out3) NOR4in

NOR4 (Vdd Vss inB S0 SBar1 SBar2 out4) NOR4in

NOR5 (Vdd Vss inB SBar0 SBar1 SBar2 out5) NOR4in

Inv (Vdd Vss in inB) bcInverter

mult=4

I0 (Vdd Vss S0 SBar0) bcInverter

mult=4

I1 (Vdd Vss S1 SBar1) bcInverter

mult=4

I2 (Vdd Vss S2 SBar2) bcInverter

mult=4

ends deMUX16

//16 bit 1:6 DEMUX

// View name: schematic

//A=out0, B=out1... F=out5

//width = 3510um

subckt deMUX16b16 Vdd Vss in0 in1 in2 in3 in4 in5 in6 in7 in8 in9 in10 in11 in12 in13 in14 in15\

S0 S1 S2 A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10 A11 A12 A13 A14 A15 \

B0 B1 B2 B3 B4 B5 B6 B7 B8 B9 B10 B11 B12 B13 B14 B15 C0 C1 C2 C3 C4 \

C5 C6 C7 C8 C9 C10 C11 C12 C13 C14 C15 D0 D1 D2 D3 D4 D5 D6 D7 \

D8 D9 D10 D11 D12 D13 D14 D15 E0 E1 E2 E3 E4 E5 E6 E7 E8 E9 E10 E11 \

E12 E13 E14 E15 F0 F1 F2 F3 F4 F5 F6 F7 F8 F9 F10 F11 F12 F13 F14 F15

I15 (Vdd Vss in15 S0 S1 S2 A15 B15 C15 D15 E15 F15) deMUX16

I14 (Vdd Vss in14 S0 S1 S2 A14 B14 C14 D14 E14 F14) deMUX16

I13 (Vdd Vss in13 S0 S1 S2 A13 B13 C13 D13 E13 F13) deMUX16

I12 (Vdd Vss in12 S0 S1 S2 A12 B12 C12 D12 E12 F12) deMUX16

I11 (Vdd Vss in11 S0 S1 S2 A11 B11 C11 D11 E11 F11) deMUX16

I10 (Vdd Vss in10 S0 S1 S2 A10 B10 C10 D10 E10 F10) deMUX16

I9 (Vdd Vss in9 S0 S1 S2 A9 B9 C9 D9 E9 F9) deMUX16

I8 (Vdd Vss in8 S0 S1 S2 A8 B8 C8 D8 E8 F8) deMUX16

I7 (Vdd Vss in7 S0 S1 S2 A7 B7 C7 D7 E7 F7) deMUX16

I6 (Vdd Vss in6 S0 S1 S2 A6 B6 C6 D6 E6 F6) deMUX16

I5 (Vdd Vss in5 S0 S1 S2 A5 B5 C5 D5 E5 F5) deMUX16

I4 (Vdd Vss in4 S0 S1 S2 A4 B4 C4 D4 E4 F4) deMUX16

I3 (Vdd Vss in3 S0 S1 S2 A3 B3 C3 D3 E3 F3) deMUX16

I2 (Vdd Vss in2 S0 S1 S2 A2 B2 C2 D2 E2 F2) deMUX16

I1 (Vdd Vss in1 S0 S1 S2 A1 B1 C1 D1 E1 F1) deMUX16

I0 (Vdd Vss in0 S0 S1 S2 A0 B0 C0 D0 E0 F0) deMUX16

ends deMUX16b16

//1:5 DEMUX for B

//This DeMUX has following pass signals (S2,S1,S0):

// out0=(0,1,X)

// out1=(1,0,0)

// out2=(1,0,1)

// out3=(1,1,0)

// out4=(1,1,1)

//width = 219.375

subckt deMUX15 (Vdd Vss in S0 S1 S2 out0 out1 out2 out3 out4)

NOR0 (Vdd Vss inB SBar1 S2 out0) NOR3in

NOR1 (Vdd Vss inB S0 S1 SBar2 out1) NOR4in

NOR2 (Vdd Vss inB SBar0 S1 SBar2 out2) NOR4in

NOR3 (Vdd Vss inB S0 SBar1 SBar2 out3) NOR4in

NOR4 (Vdd Vss inB SBar0 SBar1 SBar2 out4) NOR4in

Inv (Vdd Vss in inB) bcInverter mult=4

I0 (Vdd Vss S0 SBar0) bcInverter

mult=4

I1 (Vdd Vss S1 SBar1) bcInverter

mult=4

I2 (Vdd Vss S2 SBar2) bcInverter

mult=4

ends deMUX15

//1:4 DEMUX for B

//This DeMUX has following pass signals (S2,S1,S0):

// out0=(0,1,X) // out1=(1,0,1)

// out2=(1,1,0)

// out3=(1,1,1)

//width = 183.375um

subckt deMUX14 (Vdd Vss in S0 S1 S2 out0 out1 out2 out3)

NOR0 (Vdd Vss inB SBar1 S2 out0) NOR3in

NOR1 (Vdd Vss inB SBar0 S1 SBar2 out1) NOR4in

NOR2 (Vdd Vss inB S0 SBar1 SBar2 out2) NOR4in

NOR3 (Vdd Vss inB SBar0 SBar1 SBar2 out3) NOR4in

Inv (Vdd Vss in inB) bcInverter

mult=4

I0 (Vdd Vss S0 SBar0) bcInverter

mult=4

I1 (Vdd Vss S1 SBar1) bcInverter

mult=4

I2 (Vdd Vss S2 SBar2) bcInverter

mult=4

ends deMUX14

//16 bit DEMUX

for B inputs

// View name: schematic

//A=out0, B=out1... F=out5

//width = 3006um

subckt deMUX16b16B Vdd Vss in0 in1 in2 in3 in4 in5 in6 in7 in8 in9 in10 in11 in12 in13 in14 in15\

S0 S1 S2 B0 B1 B2 B3 B4 B5 B6 B7 B8 B9 B10 B11 B12 B13 B14 B15 C0 C1 D0 D1 D2 D3 D4 D5 D6 D7 \

D8 D9 D10 D11 D12 D13 D14 D15 E0 E1 E2 E3 E4 E5 E6 E7 E8 E9 E10 E11 \

E12 E13 E14 E15 F0 F1 F2 F3 F4 F5 F6 F7 F8 F9 F10 F11 F12 F13 F14 F15

I15 (Vdd Vss in15 S0 S1 S2 B15 D15 E15 F15) deMUX14

I14 (Vdd Vss in14 S0 S1 S2 B14 D14 E14 F14) deMUX14

I13 (Vdd Vss in13 S0 S1 S2 B13 D13 E13 F13) deMUX14

I12 (Vdd Vss in12 S0 S1 S2 B12 D12 E12 F12) deMUX14

I11 (Vdd Vss in11 S0 S1 S2 B11 D11 E11 F11) deMUX14

I10 (Vdd Vss in10 S0 S1 S2 B10 D10 E10 F10) deMUX14

I9 (Vdd Vss in9 S0 S1 S2 B9 D9 E9 F9) deMUX14

I8 (Vdd Vss in8 S0 S1 S2 B8 D8 E8 F8) deMUX14

I7 (Vdd Vss in7 S0 S1 S2 B7 D7 E7 F7) deMUX14

I6 (Vdd Vss in6 S0 S1 S2 B6 D6 E6 F6) deMUX14

I5 (Vdd Vss in5 S0 S1 S2 B5 D5 E5 F5) deMUX14

I4 (Vdd Vss in4 S0 S1 S2 B4 D4 E4 F4) deMUX14

I3 (Vdd Vss in3 S0 S1 S2 B3 D3 E3 F3) deMUX14

I2 (Vdd Vss in2 S0 S1 S2 B2 D2 E2 F2) deMUX14

I1 (Vdd Vss in1 S0 S1 S2 B1 C1 D1 E1 F1) deMUX15

I0 (Vdd Vss in0 S0 S1 S2 B0 C0 D0 E0 F0) deMUX15

ends deMUX16b16B

///////////

//PASS A://

///////////////////////////////////////////////////////////////////////////////////////////////////////////

// Library name: Project

// Cell name: PassA

// View name: schematic

//width = 6.75um

subckt PassA Ain Aout VDD VSS

I1 (VDD VSS Abuff Aout) bcInverter

I0 (VDD VSS Ain Abuff) bcInverter

ends PassA

// End of subcircuit definition.

// Library name: Project

// Cell name: PassA16

// View name: schematic

//width = 108um

subckt PassA16 VDD VSS in0 in1 in2 in3 in4 in5 in6 in7 in8 \

in9 in10 in11 in12 in13 in14 in15 out0 out1 out2 out3 out4 \

out5 out6 out7 out8 out9 out10 out11 out12 out13 out14 out15

I15 (in15 out15 VDD VSS) PassA

I14 (in14 out14 VDD VSS) PassA

I13 (in13 out13 VDD VSS) PassA

I12 (in12 out12 VDD VSS) PassA

I11 (in11 out11 VDD VSS) PassA

I10 (in10 out10 VDD VSS) PassA

I9 (in9 out9 VDD VSS) PassA

I8 (in8 out8 VDD VSS) PassA

I7 (in7 out7 VDD VSS) PassA

I6 (in6 out6 VDD VSS) PassA

I5 (in5 out5 VDD VSS) PassA

I4 (in4 out4 VDD VSS) PassA

I3 (in3 out3 VDD VSS) PassA

I2 (in2 out2 VDD VSS) PassA

I1 (in1 out1 VDD VSS) PassA

I0 (in0 out0 VDD VSS) PassA

ends PassA16

// End of subcircuit definition.

//////////////

//REGISTERS://

//////////////////////////////////////////////////////////////////////////////////////////////////////////////

// Library name: Project

// Cell name: 1bReg

// View name: schematic

//width = 55.5um

subckt Reg1b CLK D Q VDD VSS

Master (VSS VDD D Qm CLK Qm) MUX21

Slave (VSS VDD Q Qm CLK Q) MUX21

ends Reg1b

// End of subcircuit definition.

// Library name: Project

// Cell name: 16bRegister

// View name: schematic

//width = 888um

subckt Register16b VDD VSS CLK D0 D1 D2 D3 D4 D5\

D6 D7 D8 D9 D10 D11 D12 D13 D14 D15 Q0 Q1 Q2 Q3\

Q4 Q5 Q6 Q7 Q8 Q9 Q10 Q11 Q12 Q13 Q14 Q15

I15 (CLK D15 Q15 VDD VSS) Reg1b

I14 (CLK D14 Q14 VDD VSS) Reg1b

I13 (CLK D13 Q13 VDD VSS) Reg1b

I12 (CLK D12 Q12 VDD VSS) Reg1b

I11 (CLK D11 Q11 VDD VSS) Reg1b

I10 (CLK D10 Q10 VDD VSS) Reg1b

I9 (CLK D9 Q9 VDD VSS) Reg1b

I8 (CLK D8 Q8 VDD VSS) Reg1b

I7 (CLK D7 Q7 VDD VSS) Reg1b

I6 (CLK D6 Q6 VDD VSS) Reg1b

I5 (CLK D5 Q5 VDD VSS) Reg1b

I4 (CLK D0 Q0 VDD VSS) Reg1b

I3 (CLK D1 Q1 VDD VSS) Reg1b

I2 (CLK D4 Q4 VDD VSS) Reg1b

I1 (CLK D3 Q3 VDD VSS) Reg1b

I0 (CLK D2 Q2 VDD VSS) Reg1b

ends Register16b

/////////////////////

//NOR and OR GATES://

/////////////////////////////////////////////////////////////////////////////////////////////////////////

//2in NOR

subckt NOR2in Vdd Vss inA inB out

parameters wp=2\*r\*1.5u wn=1.5u ln=600n lp=600n mult=1

MPA (netAB inA Vdd Vdd) ami06P w=wp l=lp as=1.5u\*wp ad=1.5u\*wp ps=3u+wp \

pd=3u+wp m=mult region=sat

MPB (out inB netAB Vdd) ami06P w=wp l=lp as=1.5u\*wp ad=1.5u\*wp ps=3u+wp \

pd=3u+wp m=mult region=sat

MNA (out inA Vss Vss) ami06N w=wn l=ln as=1.5u\*wn ad=1.5u\*wn ps=3u+wn \

pd=3u+wn m=mult region=sat

MNB (out inB Vss Vss) ami06N w=wn l=ln as=1.5u\*wn ad=1.5u\*wn ps=3u+wn \

pd=3u+wn m=mult region=sat

ends NOR2in

//2 input OR Gate

//width = 13.875um

subckt OR2in Vdd Vss inA inB out

parameters wpA=r\*1.5u wnA=2\*1.5u multA=1

NOR (Vdd Vss inA inB outbar) NOR2in wp=wpA wn=wnA mult=multA

Inv (Vdd Vss outbar out) bcInverter mult=multA

ends OR2in

//16 bit 2 input OR Gate

//width = 222um

subckt OR2in16b Vdd Vss inA0 inA1 inA2 inA3 inA4 inA5 inA6 inA7 inA8 inA9\

inA10 inA11 inA12 inA13 inA14 inA15 inB0 inB1 inB2 inB3 inB4 inB5 inB6 inB7\

inB8 inB9 inB10 inB11 inB12 inB13 inB14 inB15 out0 out1 out2 out3 out4 out5\

out6 out7 out8 out9 out10 out11 out12 out13 out14 out15

OR0 (Vdd Vss inA0 inB0 out0) OR2in

OR1 (Vdd Vss inA1 inB1 out1) OR2in

OR2 (Vdd Vss inA2 inB2 out2) OR2in

OR3 (Vdd Vss inA3 inB3 out3) OR2in

OR4 (Vdd Vss inA4 inB4 out4) OR2in

OR5 (Vdd Vss inA5 inB5 out5) OR2in

OR6 (Vdd Vss inA6 inB6 out6) OR2in

OR7 (Vdd Vss inA7 inB7 out7) OR2in

OR8 (Vdd Vss inA8 inB8 out8) OR2in

OR9 (Vdd Vss inA9 inB9 out9) OR2in

OR10 (Vdd Vss inA10 inB10 out10) OR2in

OR11 (Vdd Vss inA11 inB11 out11) OR2in

OR12 (Vdd Vss inA12 inB12 out12) OR2in

OR13 (Vdd Vss inA13 inB13 out13) OR2in

OR14 (Vdd Vss inA14 inB14 out14) OR2in

OR15 (Vdd Vss inA15 inB15 out15) OR2in

ends OR2in16b

//3in NOR

//width = 21.375um

subckt NOR3in Vdd Vss inA inB inC out

parameters wp=3\*r\*1.5u wn=1.5u ln=600n lp=600n mult=1

MPA (netAB inA Vdd Vdd) ami06P w=wp l=lp as=1.5u\*wp ad=1.5u\*wp ps=3u+wp \

pd=3u+wp m=mult region=sat

MPB (netBC inB netAB Vdd) ami06P w=wp l=lp as=1.5u\*wp ad=1.5u\*wp ps=3u+wp \

pd=3u+wp m=mult region=sat

MPC (out inC netBC Vdd) ami06P w=wp l=lp as=1.5u\*wp ad=1.5u\*wp ps=3u+wp \

pd=3u+wp m=mult region=sat

MNA (out inA Vss Vss) ami06N w=wn l=ln as=1.5u\*wn ad=1.5u\*wn ps=3u+wn \

pd=3u+wn m=mult region=sat

MNB (out inB Vss Vss) ami06N w=wn l=ln as=1.5u\*wn ad=1.5u\*wn ps=3u+wn \

pd=3u+wn m=mult region=sat

MNC (out inC Vss Vss) ami06N w=wn l=ln as=1.5u\*wn ad=1.5u\*wn ps=3u+wn \

pd=3u+wn m=mult region=sat

ends NOR3in

//4in NOR

// width = 36um

subckt NOR4in Vdd Vss inA inB inC inD out

parameters wp=4\*r\*1.5u wn=1.5u ln=600n lp=600n mult=1

MPA (netAB inA Vdd Vdd) ami06P w=wp l=lp as=1.5u\*wp ad=1.5u\*wp ps=3u+wp \

pd=3u+wp m=mult region=sat

MPB (netBC inB netAB Vdd) ami06P w=wp l=lp as=1.5u\*wp ad=1.5u\*wp ps=3u+wp \

pd=3u+wp m=mult region=sat

MPC (netCD inC netBC Vdd) ami06P w=wp l=lp as=1.5u\*wp ad=1.5u\*wp ps=3u+wp \

pd=3u+wp m=mult region=sat

MPD (out inD netCD Vdd) ami06P w=wp l=lp as=1.5u\*wp ad=1.5u\*wp ps=3u+wp \

pd=3u+wp m=mult region=sat

MNA (out inA Vss Vss) ami06N w=wn l=ln as=1.5u\*wn ad=1.5u\*wn ps=3u+wn \

pd=3u+wn m=mult region=sat

MNB (out inB Vss Vss) ami06N w=wn l=ln as=1.5u\*wn ad=1.5u\*wn ps=3u+wn \

pd=3u+wn m=mult region=sat

MNC (out inC Vss Vss) ami06N w=wn l=ln as=1.5u\*wn ad=1.5u\*wn ps=3u+wn \

pd=3u+wn m=mult region=sat

MND (out inD Vss Vss) ami06N w=wn l=ln as=1.5u\*wn ad=1.5u\*wn ps=3u+wn \

pd=3u+wn m=mult region=sat

ends NOR4in

///////////////////////

//NAND and AND GATES://

///////////////////////////////////////////////////////////////////////////////////////////////////////////

//2in NAND

subckt NAND2in Vdd Vss inA inB out

parameters wp=r\*1.5u wn=2\*1.5u ln=600n lp=600n mult=1

MPA (out inA Vdd Vdd) ami06P w=wp l=lp as=1.5u\*wp ad=1.5u\*wp ps=3u+wp \

pd=3u+wp m=mult region=sat

MPB (out inB Vdd Vdd) ami06P w=wp l=lp as=1.5u\*wp ad=1.5u\*wp ps=3u+wp \

pd=3u+wp m=mult region=sat

MNA (out inA netAB Vss) ami06N w=wn l=ln as=1.5u\*wn ad=1.5u\*wn ps=3u+wn \

pd=3u+wn m=mult region=sat

MNB (netAB inB Vss Vss) ami06N w=wn l=ln as=1.5u\*wn ad=1.5u\*wn ps=3u+wn \

pd=3u+wn m=mult region=sat

ends NAND2in

//2 input AND Gate

// width = 16.5um

subckt AND2in Vdd Vss inA inB out

parameters wpA=r\*1.5u wnA=2\*1.5u multA=1

NAND (Vdd Vss inA inB outbar) NAND2in wp=wpA wn=wnA mult=multA

Inv (Vdd Vss outbar out) bcInverter mult=multA

ends AND2in

//16 bit 2 input AND Gate

//width = 264um

subckt AND2in16b Vdd Vss inA0 inA1 inA2 inA3 inA4 inA5 inA6 inA7 inA8 inA9\

inA10 inA11 inA12 inA13 inA14 inA15 inB0 inB1 inB2 inB3 inB4 inB5 inB6 inB7\

inB8 inB9 inB10 inB11 inB12 inB13 inB14 inB15 out0 out1 out2 out3 out4 out5\

out6 out7 out8 out9 out10 out11 out12 out13 out14 out15

AND0 (Vdd Vss inA0 inB0 out0) AND2in

AND1 (Vdd Vss inA1 inB1 out1) AND2in

AND2 (Vdd Vss inA2 inB2 out2) AND2in

AND3 (Vdd Vss inA3 inB3 out3) AND2in

AND4 (Vdd Vss inA4 inB4 out4) AND2in

AND5 (Vdd Vss inA5 inB5 out5) AND2in

AND6 (Vdd Vss inA6 inB6 out6) AND2in

AND7 (Vdd Vss inA7 inB7 out7) AND2in

AND8 (Vdd Vss inA8 inB8 out8) AND2in

AND9 (Vdd Vss inA9 inB9 out9) AND2in

AND10 (Vdd Vss inA10 inB10 out10) AND2in

AND11 (Vdd Vss inA11 inB11 out11) AND2in

AND12 (Vdd Vss inA12 inB12 out12) AND2in

AND13 (Vdd Vss inA13 inB13 out13) AND2in

AND14 (Vdd Vss inA14 inB14 out14) AND2in

AND15 (Vdd Vss inA15 inB15 out15) AND2in

ends AND2in16b

////////////////////////

//ADDER and SUBTRACTOR//

////////////////////////////////////////////////////////////////////////////////////////////////////////////

// Library name: Project

// Cell name: Adder1bInv

// View name: schematic

//width = 131.625um

subckt Adder1bInv Cin Cout S VDD VSS inA inB

parameters wp=r\*1.5u wn=1.5u ln=600n lp=600n mult=1

inAInv (VDD VSS inA inABar) bcInverter

inBInv (VDD VSS inB inBBar) bcInverter

MPA2S (PmosABS inABar VDD VDD) ami06P w=3\*wp l=lp as=1.5u\*3\*wp ad=1.5u\*3\*wp ps=3u+3\*wp \

pd=3u+3\*wp m=mult region=sat

MPB2S (PmosBCinS inBBar PmosABS VDD) ami06P w=3\*wp l=lp as=1.5u\*wp ad=1.5u\*3\*wp ps=3u+3\*wp \

pd=3u+wp m=mult region=sat

MPCin2S (S Cin PmosBCinS VDD) ami06P w=3\*wp l=lp as=1.5u\*3\*wp ad=1.5u\*3\*wp ps=3u+3\*wp \

pd=3u+3\*wp m=mult region=sat

MPB1S (PmosS1 inBBar VDD VDD) ami06P w=2\*wp l=lp as=1.5u\*2\*wp ad=1.5u\*2\*wp ps=3u+2\*wp \

pd=3u+2\*wp m=mult region=sat

MPA1S (PmosS1 inABar VDD VDD) ami06P w=2\*wp l=lp as=1.5u\*2\*wp ad=1.5u\*2\*wp ps=3u+2\*wp \

pd=3u+2\*wp m=mult region=sat

MPCin1S (PmosS1 Cin VDD VDD) ami06P w=2\*wp l=lp as=1.5u\*2\*wp ad=1.5u\*2\*wp ps=3u+2\*wp \

pd=3u+2\*wp m=mult region=sat

MPCoutS (S Cout PmosS1 VDD) ami06P w=2\*wp l=lp as=1.5u\*2\*wp ad=1.5u\*2\*wp ps=3u+2\*wp \

pd=3u+2\*wp m=mult region=sat

MPA2Cout (PmosAB2 inABar VDD VDD) ami06P w=2\*wp l=lp as=1.5u\*2\*wp ad=1.5u\*2\*wp ps=3u+2\*wp \

pd=3u+2\*wp m=mult region=sat

MPB2Cout (Cout inBBar PmosAB2 VDD) ami06P w=2\*wp l=lp as=1.5u\*2\*wp ad=1.5u\*2\*wp ps=3u+2\*wp \

pd=3u+2\*wp m=mult region=sat

MPB1Cout (PmosABCin1 inBBar VDD VDD) ami06P w=6\*wp l=lp as=1.5u\*6\*wp ad=1.5u\*6\*wp ps=3u+6\*wp \

pd=3u+6\*wp m=mult region=sat

MPA1Cout (PmosABCin1 inABar VDD VDD) ami06P w=6\*wp l=lp as=1.5u\*6\*wp ad=1.5u\*6\*wp ps=3u+6\*wp \

pd=3u+6\*wp m=mult region=sat

MPCinCout (Cout Cin PmosABCin1 VDD) ami06P w=6\*wp l=lp as=1.5u\*6\*wp ad=1.5u\*6\*wp ps=3u+6\*wp \

pd=3u+6\*wp m=mult region=sat

MNB2S (NmosABS inBBar VSS VSS) ami06N w=3\*wn l=ln as=1.5u\*3\*wn ad=1.5u\*3\*wn ps=3u+3\*wn \

pd=3u+3\*wn m=mult region=sat

MNA2S (NmosBCinS inABar NmosABS VSS) ami06N w=3\*wn l=ln as=1.5u\*3\*wn ad=1.5u\*3\*wn ps=3u+3\*wn \

pd=3u+3\*wn m=mult region=sat

MNCin2S (S Cin NmosBCinS VSS) ami06N w=3\*wn l=ln as=1.5u\*3\*wn ad=1.5u\*3\*wn ps=3u+3\*wn \

pd=3u+3\*wn m=mult region=sat

MNCoutS (S Cout NmosS1 VSS) ami06N w=2\*wn l=ln as=1.5u\*2\*wn ad=1.5u\*2\*wn ps=3u+2\*wn \

pd=3u+2\*wn m=mult region=sat

MNCin1S (NmosS1 Cin VSS VSS) ami06N w=2\*wn l=ln as=1.5u\*2\*wn ad=1.5u\*2\*wn ps=3u+2\*wn \

pd=3u+2\*wn m=mult region=sat

MNB1S (NmosS1 inBBar VSS VSS) ami06N w=2\*wn l=ln as=1.5u\*2\*wn ad=1.5u\*2\*wn ps=3u+2\*wn \

pd=3u+2\*wn m=mult region=sat

MNA1S (NmosS1 inABar VSS VSS) ami06N w=2\*wn l=ln as=1.5u\*2\*wn ad=1.5u\*2\*wn ps=3u+2\*wn \

pd=3u+2\*wn m=mult region=sat

MNA2Cout (Cout inABar NmosAB2 VSS) ami06N w=2\*wn l=ln as=1.5u\*2\*wn ad=1.5u\*2\*wn ps=3u+2\*wn \

pd=3u+2\*wn m=mult region=sat

MNB2Cout (NmosAB2 inBBar VSS VSS) ami06N w=2\*wn l=ln as=1.5u\*2\*wn ad=1.5u\*2\*wn ps=3u+2\*wn \

pd=3u+2\*wn m=mult region=sat

MNB1Cout (NmosABCin1 inBBar VSS VSS) ami06N w=6\*wn l=ln as=1.5u\*6\*wn ad=1.5u\*6\*wn ps=3u+6\*wn \

pd=3u+6\*wn m=mult region=sat

MNA1Cout (NmosABCin1 inABar VSS VSS) ami06N w=6\*wn l=ln as=1.5u\*6\*wn ad=1.5u\*6\*wn ps=3u+6\*wn \

pd=3u+wn m=mult region=sat

MNCinCout (Cout Cin NmosABCin1 VSS) ami06N w=6\*wn l=ln as=1.5u\*6\*wn ad=1.5u\*6\*wn ps=3u+6\*wn \

pd=3u+wn m=mult region=sat

ends Adder1bInv

// End of subcircuit definition.

// Library name: Project

// Cell name: Adder1bNInv

// View name: schematic

//width = 135um

subckt Adder1bNInv Cin Cout S VDD VSS inA inB

parameters wp=r\*1.5u wn=1.5u ln=600n lp=600n mult=1

SumInv (VDD VSS SBar S) bcInverter

MPA2S (PmosABS inA VDD VDD) ami06P w=3\*wp l=lp as=1.5u\*3\*wp ad=1.5u\*3\*wp ps=3u+3\*wp \

pd=3u+3\*wp m=mult region=sat

MPB2S (PmosBCinS inB PmosABS VDD) ami06P w=3\*wp l=lp as=1.5u\*wp ad=1.5u\*3\*wp ps=3u+3\*wp \

pd=3u+wp m=mult region=sat

MPCin2S (SBar Cin PmosBCinS VDD) ami06P w=3\*wp l=lp as=1.5u\*3\*wp ad=1.5u\*3\*wp ps=3u+3\*wp \

pd=3u+3\*wp m=mult region=sat

MPB1S (PmosS1 inB VDD VDD) ami06P w=2\*wp l=lp as=1.5u\*2\*wp ad=1.5u\*2\*wp ps=3u+2\*wp \

pd=3u+2\*wp m=mult region=sat

MPA1S (PmosS1 inA VDD VDD) ami06P w=2\*wp l=lp as=1.5u\*2\*wp ad=1.5u\*2\*wp ps=3u+2\*wp \

pd=3u+2\*wp m=mult region=sat

MPCin1S (PmosS1 Cin VDD VDD) ami06P w=2\*wp l=lp as=1.5u\*2\*wp ad=1.5u\*2\*wp ps=3u+2\*wp \

pd=3u+2\*wp m=mult region=sat

MPCoutS (SBar Cout PmosS1 VDD) ami06P w=2\*wp l=lp as=1.5u\*2\*wp ad=1.5u\*2\*wp ps=3u+2\*wp \

pd=3u+2\*wp m=mult region=sat

MPA2Cout (PmosAB2 inA VDD VDD) ami06P w=2\*wp l=lp as=1.5u\*2\*wp ad=1.5u\*2\*wp ps=3u+2\*wp \

pd=3u+2\*wp m=mult region=sat

MPB2Cout (Cout inB PmosAB2 VDD) ami06P w=2\*wp l=lp as=1.5u\*2\*wp ad=1.5u\*2\*wp ps=3u+2\*wp \

pd=3u+2\*wp m=mult region=sat

MPB1Cout (PmosABCin1 inB VDD VDD) ami06P w=6\*wp l=lp as=1.5u\*6\*wp ad=1.5u\*6\*wp ps=3u+6\*wp \

pd=3u+6\*wp m=mult region=sat

MPA1Cout (PmosABCin1 inA VDD VDD) ami06P w=6\*wp l=lp as=1.5u\*6\*wp ad=1.5u\*6\*wp ps=3u+6\*wp \

pd=3u+6\*wp m=mult region=sat

MPCinCout (Cout Cin PmosABCin1 VDD) ami06P w=6\*wp l=lp as=1.5u\*6\*wp ad=1.5u\*6\*wp ps=3u+6\*wp \

pd=3u+6\*wp m=mult region=sat

MNB2S (NmosABS inB VSS VSS) ami06N w=3\*wn l=ln as=1.5u\*3\*wn ad=1.5u\*3\*wn ps=3u+3\*wn \

pd=3u+3\*wn m=mult region=sat

MNA2S (NmosBCinS inA NmosABS VSS) ami06N w=3\*wn l=ln as=1.5u\*3\*wn ad=1.5u\*3\*wn ps=3u+3\*wn \

pd=3u+3\*wn m=mult region=sat

MNCin2S (SBar Cin NmosBCinS VSS) ami06N w=3\*wn l=ln as=1.5u\*3\*wn ad=1.5u\*3\*wn ps=3u+3\*wn \

pd=3u+3\*wn m=mult region=sat

MNCoutS (SBar Cout NmosS1 VSS) ami06N w=2\*wn l=ln as=1.5u\*2\*wn ad=1.5u\*2\*wn ps=3u+2\*wn \

pd=3u+2\*wn m=mult region=sat

MNCin1S (NmosS1 Cin VSS VSS) ami06N w=2\*wn l=ln as=1.5u\*2\*wn ad=1.5u\*2\*wn ps=3u+2\*wn \

pd=3u+2\*wn m=mult region=sat

MNB1S (NmosS1 inB VSS VSS) ami06N w=2\*wn l=ln as=1.5u\*2\*wn ad=1.5u\*2\*wn ps=3u+2\*wn \

pd=3u+2\*wn m=mult region=sat

MNA1S (NmosS1 inA VSS VSS) ami06N w=2\*wn l=ln as=1.5u\*2\*wn ad=1.5u\*2\*wn ps=3u+2\*wn \

pd=3u+2\*wn m=mult region=sat

MNA2Cout (Cout inA NmosAB2 VSS) ami06N w=2\*wn l=ln as=1.5u\*2\*wn ad=1.5u\*2\*wn ps=3u+2\*wn \

pd=3u+2\*wn m=mult region=sat

MNB2Cout (NmosAB2 inB VSS VSS) ami06N w=2\*wn l=ln as=1.5u\*2\*wn ad=1.5u\*2\*wn ps=3u+2\*wn \

pd=3u+2\*wn m=mult region=sat

MNB1Cout (NmosABCin1 inB VSS VSS) ami06N w=6\*wn l=ln as=1.5u\*6\*wn ad=1.5u\*6\*wn ps=3u+6\*wn \

pd=3u+6\*wn m=mult region=sat

MNA1Cout (NmosABCin1 inA VSS VSS) ami06N w=6\*wn l=ln as=1.5u\*6\*wn ad=1.5u\*6\*wn ps=3u+6\*wn \

pd=3u+wn m=mult region=sat

MNCinCout (Cout Cin NmosABCin1 VSS) ami06N w=6\*wn l=ln as=1.5u\*6\*wn ad=1.5u\*6\*wn ps=3u+6\*wn \

pd=3u+wn m=mult region=sat

ends Adder1bNInv

// End of subcircuit definition.

// Library name: Project

// Cell name: 16bAdder

// View name: schematic

// width =

2133um

subckt Adder16b Vdd Vss inA0 inA1 inA2 inA3 inA4 inA5 inA6 inA7 inA8 inA9\

inA10 inA11 inA12 inA13 inA14 inA15 inB0 inB1 inB2 inB3 inB4 inB5 inB6 inB7\

inB8 inB9 inB10 inB11 inB12 inB13 inB14 inB15 Cin Cout S0 S1 S2 S3 S4 S5 S6\

S7 S8 S9 S10 S11 S12 S13 S14 S15

I15 (Cout14 Cout S15 Vdd Vss inA15 inB15) Adder1bInv

I14 (Cout10 Cout11 S11 Vdd Vss inA11 inB11) Adder1bInv

I13 (Cout6 Cout7 S7 Vdd Vss inA7 inB7) Adder1bInv

I12 (Cout2 Cout3 S3 Vdd Vss inA3 inB3) Adder1bInv

I11 (Cout12 Cout13 S13 Vdd Vss inA13 inB13) Adder1bInv

I10 (Cout8 Cout9 S9 Vdd Vss inA9 inB9) Adder1bInv

I9 (Cout4 Cout5 S5 Vdd Vss inA5 inB5) Adder1bInv

I8 (Cout0 Cout1 S1 Vdd Vss inA1 inB1) Adder1bInv

I7 (Cout13 Cout14 S14 Vdd Vss inA14 inB14) Adder1bNInv

I6 (Cout9 Cout10 S10 Vdd Vss inA10 inB10) Adder1bNInv

I5 (Cout5 Cout6 S6 Vdd Vss inA6 inB6) Adder1bNInv

I4 (Cout1 Cout2 S2 Vdd Vss inA2 inB2) Adder1bNInv

I3 (Cout11 Cout12 S12 Vdd Vss inA12 inB12) Adder1bNInv

I2 (Cout7 Cout8 S8 Vdd Vss inA8 inB8) Adder1bNInv

I1 (Cout3 Cout4 S4 Vdd Vss inA4 inB4) Adder1bNInv

I0 (Cin Cout0 S0 Vdd Vss inA0 inB0) Adder1bNInv

ends Adder16b

//Cell name: subtractor/adder

//Sel=0 is Add, Sel=1 is Subtract

//This gate has no Cin input

//width = 2631

subckt SubAdd16b Vdd Vss Sel inA0 inA1 inA2 inA3 inA4 inA5 inA6 inA7 inA8 inA9\

inA10 inA11 inA12 inA13 inA14 inA15 inB0 inB1 inB2 inB3 inB4 inB5\

inB6 inB7 inB8 inB9 inB10 inB11 inB12 inB13 inB14 inB15 Cout\

S0 S1 S2 S3 S4 S5 S6 S7 S8 S9 S10 S11 S12 S13 S14 S15

MUXSelect (Vdd Vss inB0 inB1 inB2 inB3 inB4 inB5 inB6 inB7 inB8 inB9\

inB10 inB11 inB12 inB13 inB14 inB15 inBbar0\

inBbar1 inBbar2 inBbar3 inBbar4 inBbar5 inBbar6\

inBbar7 inBbar8 inBbar9 inBbar10 inBbar11 inBbar12\

inBbar13 inBbar14 inBbar15 Sel inputB0 inputB1 inputB2\

inputB3 inputB4 inputB5 inputB6 inputB7 inputB8 inputB9\

inputB10 inputB11 inputB12 inputB13 inputB14 inputB15) MUX16b21

I0 (Vdd Vss inB0 inBbar0) bcInverter

I1 (Vdd Vss inB1 inBbar1) bcInverter

I2 (Vdd Vss inB2 inBbar2) bcInverter

I3 (Vdd Vss inB3 inBbar3) bcInverter

I4 (Vdd Vss inB4 inBbar4) bcInverter

I5 (Vdd Vss inB5 inBbar5) bcInverter

I6 (Vdd Vss inB6 inBbar6) bcInverter

I7 (Vdd Vss inB7 inBbar7) bcInverter

I8 (Vdd Vss inB8 inBbar8) bcInverter

I9 (Vdd Vss inB9 inBbar9) bcInverter

I10 (Vdd Vss inB10 inBbar10) bcInverter

I11 (Vdd Vss inB11 inBbar11) bcInverter

I12 (Vdd Vss inB12 inBbar12) bcInverter

I13 (Vdd Vss inB13 inBbar13) bcInverter

I14 (Vdd Vss inB14 inBbar14) bcInverter

I15 (Vdd Vss inB15 inBbar15) bcInverter

Adder (Vdd Vss inA0 inA1 inA2 inA3 inA4 inA5 inA6 inA7 inA8\

inA9 inA10 inA11 inA12 inA13 inA14 inA15\

inputB0 inputB1 inputB2 inputB3 inputB4 inputB5 inputB6 inputB7 inputB8\

inputB9 inputB10 inputB11 inputB12 inputB13 inputB14 inputB15\

Sel Cout S0 S1 S2 S3 S4 S5 S6 S7 S8 S9 S10 S11 S12 S13 S14 S15) Adder16b

ends SubAdd16b

/////////////////////////////////////////////////////////////////////////////////////////////////////////

//Multiplier//

//////////////

subckt Adder1bInv2 Cin Cout S VDD VSS inA inB

AdderInv (Cin Coutb Sb VDD VSS inAb inBb) Adder1bNInv

InvA (VDD VSS inA inAb) bcInverter

InvB (VDD VSS inB inBb) bcInverter

//InvCin (VDD VSS Cin Cinb) bcInverter

InvCout (VDD VSS Coutb Cout) bcInverter

InvS (VDD VSS Sb S) bcInverter

ends Adder1bInv2

//Multiplier

// Width = 9017.625um

// Power = 29.69mW

// Delay = 12.7794nsec

subckt Mult VDD VSS InA0 InA1 InA2 InA3 InA4 InA5 InA6 InA7 InB0 InB1 InB2 InB3 InB4 InB5 InB6 InB7\

Out0 Out1 Out2 Out3 Out4 Out5 Out6 Out7 Out8 Out9 Out10 Out11 Out12 Out13 Out14 Out15

ADD0 (VSS FA0Cout0 Sum1 VDD VSS FA0inA0 FA0inB0) Adder1bInv2

ADD1 (FA0Cout0 FA0Cout1 FA1inA0 VDD VSS FA0inA1 FA0inB1) Adder1bInv2

ADD2 (FA0Cout1 FA0Cout2 FA1inA1 VDD VSS FA0inA2 FA0inB2) Adder1bInv2

ADD3 (FA0Cout2 FA0Cout3 FA1inA2 VDD VSS FA0inA3 FA0inB3) Adder1bInv2

ADD4 (FA0Cout3 FA0Cout4 FA1inA3 VDD VSS FA0inA4 FA0inB4) Adder1bInv2

ADD5 (FA0Cout4 FA0Cout5 FA1inA4 VDD VSS FA0inA5 FA0inB5) Adder1bInv2

ADD6 (FA0Cout5 FA0Cout6 FA1inA5 VDD VSS FA0inA6 FA0inB6) Adder1bInv2

ADD7 (FA0Cout6 FA1inA7b FA1inA6 VDD VSS VDD FA0inB7) Adder1bInv2

ADD8 (VSS FA1Cout0 Sum2 VDD VSS FA1inA0 FA1inB0) Adder1bInv2

ADD9 (FA1Cout0 FA1Cout1 FA2inA0 VDD VSS FA1inA1 FA1inB1) Adder1bInv2

ADD10 (FA1Cout1 FA1Cout2 FA2inA1 VDD VSS FA1inA2 FA1inB2) Adder1bInv2

ADD11 (FA1Cout2 FA1Cout3 FA2inA2 VDD VSS FA1inA3 FA1inB3) Adder1bInv2

ADD12 (FA1Cout3 FA1Cout4 FA2inA3 VDD VSS FA1inA4 FA1inB4) Adder1bInv2

ADD13 (FA1Cout4 FA1Cout5 FA2inA4 VDD VSS FA1inA5 FA1inB5) Adder1bInv2

ADD14 (FA1Cout5 FA1Cout6 FA2inA5 VDD VSS FA1inA6 FA1inB6) Adder1bInv2

ADD15 (FA1Cout6 FA2inA7b FA2inA6 VDD VSS FA1inA7 FA1inB7) Adder1bInv2

ADD16 (VSS FA2Cout0 Sum3 VDD VSS FA2inA0 FA2inB0) Adder1bInv2

ADD17 (FA2Cout0 FA2Cout1 FA3inA0 VDD VSS FA2inA1 FA2inB1) Adder1bInv2

ADD18 (FA2Cout1 FA2Cout2 FA3inA1 VDD VSS FA2inA2 FA2inB2) Adder1bInv2

ADD19 (FA2Cout2 FA2Cout3 FA3inA2 VDD VSS FA2inA3 FA2inB3) Adder1bInv2

ADD20 (FA2Cout3 FA2Cout4 FA3inA3 VDD VSS FA2inA4 FA2inB4) Adder1bInv2

ADD21 (FA2Cout4 FA2Cout5 FA3inA4 VDD VSS FA2inA5 FA2inB5) Adder1bInv2

ADD22 (FA2Cout5 FA2Cout6 FA3inA5 VDD VSS FA2inA6 FA2inB6) Adder1bInv2

ADD23 (FA2Cout6 FA3inA7b FA3inA6 VDD VSS FA2inA7 FA2inB7) Adder1bInv2

ADD24 (VSS FA3Cout0 Sum4 VDD VSS FA3inA0 FA3inB0) Adder1bInv2

ADD25 (FA3Cout0 FA3Cout1 FA4inA0 VDD VSS FA3inA1 FA3inB1) Adder1bInv2

ADD26 (FA3Cout1 FA3Cout2 FA4inA1 VDD VSS FA3inA2 FA3inB2) Adder1bInv2

ADD27 (FA3Cout2 FA3Cout3 FA4inA2 VDD VSS FA3inA3 FA3inB3) Adder1bInv2

ADD28 (FA3Cout3 FA3Cout4 FA4inA3 VDD VSS FA3inA4 FA3inB4) Adder1bInv2

ADD29 (FA3Cout4 FA3Cout5 FA4inA4 VDD VSS FA3inA5 FA3inB5) Adder1bInv2

ADD30 (FA3Cout5 FA3Cout6 FA4inA5 VDD VSS FA3inA6 FA3inB6) Adder1bInv2

ADD31 (FA3Cout6 FA4inA7b FA4inA6 VDD VSS FA3inA7 FA3inB7) Adder1bInv2

ADD32 (VSS FA4Cout0 Sum5 VDD VSS FA4inA0 FA4inB0) Adder1bInv2

ADD33 (FA4Cout0 FA4Cout1 FA5inA0 VDD VSS FA4inA1 FA4inB1) Adder1bInv2

ADD34 (FA4Cout1 FA4Cout2 FA5inA1 VDD VSS FA4inA2 FA4inB2) Adder1bInv2

ADD35 (FA4Cout2 FA4Cout3 FA5inA2 VDD VSS FA4inA3 FA4inB3) Adder1bInv2

ADD36 (FA4Cout3 FA4Cout4 FA5inA3 VDD VSS FA4inA4 FA4inB4) Adder1bInv2

ADD37 (FA4Cout4 FA4Cout5 FA5inA4 VDD VSS FA4inA5 FA4inB5) Adder1bInv2

ADD38 (FA4Cout5 FA4Cout6 FA5inA5 VDD VSS FA4inA6 FA4inB6) Adder1bInv2

ADD39 (FA4Cout6 FA5inA7b FA5inA6 VDD VSS FA4inA7 FA4inB7) Adder1bInv2

ADD40 (VSS FA5Cout0 Sum6 VDD VSS FA5inA0 FA5inB0) Adder1bInv2

ADD41 (FA5Cout0 FA5Cout1 FA6inA0 VDD VSS FA5inA1 FA5inB1) Adder1bInv2

ADD42 (FA5Cout1 FA5Cout2 FA6inA1 VDD VSS FA5inA2 FA5inB2) Adder1bInv2

ADD43 (FA5Cout2 FA5Cout3 FA6inA2 VDD VSS FA5inA3 FA5inB3) Adder1bInv2

ADD44 (FA5Cout3 FA5Cout4 FA6inA3 VDD VSS FA5inA4 FA5inB4) Adder1bInv2

ADD45 (FA5Cout4 FA5Cout5 FA6inA4 VDD VSS FA5inA5 FA5inB5) Adder1bInv2

ADD46 (FA5Cout5 FA5Cout6 FA6inA5 VDD VSS FA5inA6 FA5inB6) Adder1bInv2

ADD47 (FA5Cout6 FA6inA7b FA6inA6 VDD VSS FA5inA7 FA5inB7) Adder1bInv2

ADD48 (VSS FA6Cout0 Sum7 VDD VSS FA5inA0 FA6inB0) Adder1bInv2

ADD49 (FA6Cout0 FA6Cout1 Sum8 VDD VSS FA6inA1 FA6inB1) Adder1bInv2

ADD50 (FA6Cout1 FA6Cout2 Sum9 VDD VSS FA6inA2 FA6inB2) Adder1bInv2

ADD51 (FA6Cout2 FA6Cout3 Sum10 VDD VSS FA6inA3 FA6inB3) Adder1bInv2

ADD52 (FA6Cout3 FA6Cout4 Sum11 VDD VSS FA6inA4 FA6inB4) Adder1bInv2

ADD53 (FA6Cout4 FA6Cout5 Sum12 VDD VSS FA6inA5 FA6inB5) Adder1bInv2

ADD54 (FA6Cout5 FA6Cout6 Sum13 VDD VSS FA6inA6 FA6inB6) Adder1bInv2

ADD55 (FA6Cout6 Out15 Sum14 VDD VSS FA6inA7 FA6inB7) Adder1bInv2

NAND0 (VDD VSS InA0 InB0 Sum0) NAND2in

NAND1 (VDD VSS InA1 InB0 FA0inA0) NAND2in

NAND2 (VDD VSS InA2 InB0 FA0inA1) NAND2in

NAND3 (VDD VSS InA3 InB0 FA0inA2) NAND2in

NAND4 (VDD VSS InA4 InB0 FA0inA3) NAND2in

NAND5 (VDD VSS InA5 InB0 FA0inA4) NAND2in

NAND6 (VDD VSS InA6 InB0 FA0inA5) NAND2in

NAND7 (VDD VSS InA7 InB0 FA0inA6) NAND2in

NAND8 (VDD VSS InA0 InB1 FA0inB0) NAND2in

NAND9 (VDD VSS InA1 InB1 FA0inB1) NAND2in

NAND10 (VDD VSS InA2 InB1 FA0inB2) NAND2in

NAND11 (VDD VSS InA3 InB1 FA0inB3) NAND2in

NAND12 (VDD VSS InA4 InB1 FA0inB4) NAND2in

NAND13 (VDD VSS InA5 InB1 FA0inB5) NAND2in

NAND14 (VDD VSS InA6 InB1 FA0inB6) NAND2in

NAND15 (VDD VSS InA7 InB1 FA0inB7) NAND2in

NAND16 (VDD VSS InA0 InB2 FA1inB0) NAND2in

NAND17 (VDD VSS InA1 InB2 FA1inB1) NAND2in

NAND18 (VDD VSS InA2 InB2 FA1inB2) NAND2in

NAND19 (VDD VSS InA3 InB2 FA1inB3) NAND2in

NAND20 (VDD VSS InA4 InB2 FA1inB4) NAND2in

NAND21 (VDD VSS InA5 InB2 FA1inB5) NAND2in

NAND22 (VDD VSS InA6 InB2 FA1inB6) NAND2in

NAND23 (VDD VSS InA7 InB2 FA1inB7) NAND2in

NAND24 (VDD VSS InA0 InB3 FA2inB0) NAND2in

NAND25 (VDD VSS InA1 InB3 FA2inB1) NAND2in

NAND26 (VDD VSS InA2 InB3 FA2inB2) NAND2in

NAND27 (VDD VSS InA3 InB3 FA2inB3) NAND2in

NAND28 (VDD VSS InA4 InB3 FA2inB4) NAND2in

NAND29 (VDD VSS InA5 InB3 FA2inB5) NAND2in

NAND30 (VDD VSS InA6 InB3 FA2inB6) NAND2in

NAND31 (VDD VSS InA7 InB3 FA2inB7) NAND2in

NAND32 (VDD VSS InA0 InB4 FA3inB0) NAND2in

NAND33 (VDD VSS InA1 InB4 FA3inB1) NAND2in

NAND34 (VDD VSS InA2 InB4 FA3inB2) NAND2in

NAND35 (VDD VSS InA3 InB4 FA3inB3) NAND2in

NAND36 (VDD VSS InA4 InB4 FA3inB4) NAND2in

NAND37 (VDD VSS InA5 InB4 FA3inB5) NAND2in

NAND38 (VDD VSS InA6 InB4 FA3inB6) NAND2in

NAND39 (VDD VSS InA7 InB4 FA3inB7) NAND2in

NAND40 (VDD VSS InA0 InB5 FA4inB0) NAND2in

NAND41 (VDD VSS InA1 InB5 FA4inB1) NAND2in

NAND42 (VDD VSS InA2 InB5 FA4inB2) NAND2in

NAND43 (VDD VSS InA3 InB5 FA4inB3) NAND2in

NAND44 (VDD VSS InA4 InB5 FA4inB4) NAND2in

NAND45 (VDD VSS InA5 InB5 FA4inB5) NAND2in

NAND46 (VDD VSS InA6 InB5 FA4inB6) NAND2in

NAND47 (VDD VSS InA7 InB5 FA4inB7) NAND2in

NAND48 (VDD VSS InA0 InB6 FA5inB0) NAND2in

NAND49 (VDD VSS InA1 InB6 FA5inB1) NAND2in

NAND50 (VDD VSS InA2 InB6 FA5inB2) NAND2in

NAND51 (VDD VSS InA3 InB6 FA5inB3) NAND2in

NAND52 (VDD VSS InA4 InB6 FA5inB4) NAND2in

NAND53 (VDD VSS InA5 InB6 FA5inB5) NAND2in

NAND54 (VDD VSS InA6 InB6 FA5inB6) NAND2in

NAND55 (VDD VSS InA7 InB6 FA5inB7) NAND2in

NAND56 (VDD VSS InA0 InB7 FA6inB0) NAND2in

NAND57 (VDD VSS InA1 InB7 FA6inB1) NAND2in

NAND58 (VDD VSS InA2 InB7 FA6inB2) NAND2in

NAND59 (VDD VSS InA3 InB7 FA6inB3) NAND2in

NAND60 (VDD VSS InA4 InB7 FA6inB4) NAND2in

NAND61 (VDD VSS InA5 InB7 FA6inB5) NAND2in

NAND62 (VDD VSS InA6 InB7 FA6inB6) NAND2in

NAND63 (VDD VSS InA7 InB7 FA6inB7) NAND2in

InvC0 (VDD VSS FA1inA7b FA1inA7) bcInverter

InvC1 (VDD VSS FA2inA7b FA2inA7) bcInverter

InvC2 (VDD VSS FA3inA7b FA3inA7) bcInverter

InvC3 (VDD VSS FA4inA7b FA4inA7) bcInverter

InvC4 (VDD VSS FA5inA7b FA5inA7) bcInverter

InvC5 (VDD VSS FA6inA7b FA6inA7) bcInverter

InvC6 (VDD VSS FA7inA7b FA7inA7) bcInverter

Inv0 (VDD VSS Sum0 Out0) bcInverter

Inv1 (VDD VSS Sum1 Out1) bcInverter

Inv2 (VDD VSS Sum2 Out2) bcInverter

Inv3 (VDD VSS Sum3 Out3) bcInverter

Inv4 (VDD VSS Sum4 Out4) bcInverter

Inv5 (VDD VSS Sum5 Out5) bcInverter

Inv6 (VDD VSS Sum6 Out6) bcInverter

Inv7 (VDD VSS Sum7 Out7) bcInverter

Inv8 (VDD VSS Sum8 Out8) bcInverter

Inv9 (VDD VSS Sum9 Out9) bcInverter

Inv10 (VDD VSS Sum10 Out10) bcInverter

Inv11 (VDD VSS Sum11 Out11) bcInverter

Inv12 (VDD VSS Sum12 Out12) bcInverter

Inv13 (VDD VSS Sum13 Out13) bcInverter

Inv14 (VDD VSS Sum14 Out14) bcInverter

ends Mult

///////

//ALU//

////////////////////////////////////////////////////////////////////////////////////////////////////////////

//ALU subcircuit

//Control signals:

// 0=NoOp

// 1=Pass

// 2=Add

// 3=Subtract

// 4=Shift

// 5=And

// 6=Or

// 7=Multiply

subckt ALU Vdd Vss CLK inA0 inA1 inA2 inA3 inA4 inA5 inA6 inA7 inA8 inA9\

inA10 inA11 inA12 inA13 inA14 inA15 inB0 inB1 inB2 inB3 inB4 inB5\

inB6 inB7 inB8 inB9 inB10 inB11 inB12 inB13 inB14 inB15 S0 S1 S2\

out0 out1 out2 out3 out4 out5 out6 out7 out8 out9 out10 out11 out12\

out13 out14 out15 CoutputAdd

RegA (Vdd Vss CLK inA0 inA1 inA2 inA3 inA4 inA5 inA6 inA7 inA8 inA9\

inA10 inA11 inA12 inA13 inA14 inA15 inpA0 inpA1\

inpA2 inpA3 inpA4 inpA5 inpA6 inpA7 inpA8 inpA9 inpA10\

inpA11 inpA12 inpA13 inpA14 inpA15) Register16b

RegB (Vdd Vss CLK inB0 inB1 inB2 inB3 inB4 inB5 inB6 inB7 inB8 inB9\

inB10 inB11 inB12 inB13 inB14 inB15 inpB0 inpB1\

inpB2 inpB3 inpB4 inpB5 inpB6 inpB7 inpB8 inpB9 inpB10\

inpB11 inpB12 inpB13 inpB14 inpB15) Register16b

FirstdeMUXA (Vdd Vss inpA0 inpA1 inpA2 inpA3 inpA4 inpA5 inpA6 inpA7 inpA8 inpA9\

inpA10 inpA11 inpA12 inpA13 inpA14 inpA15 S0 S1 S2 inputAP0 inputAP1 inputAP2\

inputAP3 inputAP4 inputAP5 inputAP6 inputAP7 inputAP8 inputAP9 inputAP10\

inputAP11 inputAP12 inputAP13 inputAP14 inputAP15 inputAAddSub0 inputAAddSub1 \

inputAAddSub2 inputAAddSub3 inputAAddSub4 inputAAddSub5 inputAAddSub6\

inputAAddSub7 inputAAddSub8 inputAAddSub9 inputAAddSub10 inputAAddSub11\

inputAAddSub12 inputAAddSub13 inputAAddSub14 inputAAddSub15 inputASh0 inputASh1\

inputASh2 inputASh3 inputASh4 inputASh5 inputASh6 inputASh7 \

inputASh8 inputASh9 inputASh10 inputASh11 inputASh12 inputASh13 inputASh14\

inputASh15 inputAAnd0 inputAAnd1 inputAAnd2 inputAAnd3 inputAAnd4 inputAAnd5\

inputAAnd6 inputAAnd7 inputAAnd8 inputAAnd9 inputAAnd10 inputAAnd11 \

inputAAnd12 inputAAnd13 inputAAnd14 inputAAnd15 inputAOr0 inputAOr1 inputAOr2\

inputAOr3 inputAOr4 inputAOr5 inputAOr6 inputAOr7 inputAOr8 inputAOr9\

inputAOr10 inputAOr11 inputAOr12 inputAOr13 inputAOr14 inputAOr15 inputAMult0\

inputAMult1 inputAMult2 inputAMult3 inputAMult4 inputAMult5 inputAMult6\

inputAMult7 Vss Vss Vss Vss Vss Vss Vss Vss) deMUX16b16

FirstdeMUXB (Vdd Vss inpB0 inpB1 inpB2 inpB3 inpB4 inpB5 inpB6 inpB7 inpB8 inpB9\

inpB10 inpB11 inpB12 inpB13 inpB14 inpB15 S0 S1 S2 inputBAddSub0 inputBAddSub1 \

inputBAddSub2 inputBAddSub3 inputBAddSub4 inputBAddSub5 inputBAddSub6\

inputBAddSub7 inputBAddSub8 inputBAddSub9 inputBAddSub10 inputBAddSub11\

inputBAddSub12 inputBAddSub13 inputBAddSub14 inputBAddSub15 inputBSh0 inputBSh1\

inputBAnd0 inputBAnd1 inputBAnd2 inputBAnd3 inputBAnd4 inputBAnd5\

inputBAnd6 inputBAnd7 inputBAnd8 inputBAnd9 inputBAnd10 inputBAnd11 \

inputBAnd12 inputBAnd13 inputBAnd14 inputBAnd15 inputBOr0 inputBOr1 inputBOr2\

inputBOr3 inputBOr4 inputBOr5 inputBOr6 inputBOr7 inputBOr8 inputBOr9\

inputBOr10 inputBOr11 inputBOr12 inputBOr13 inputBOr14 inputBOr15 inputBMult0\

inputBMult1 inputBMult2 inputBMult3 inputBMult4 inputBMult5 inputBMult6\

inputBMult7 Vss Vss Vss Vss Vss Vss Vss Vss) deMUX16b16B

RegOut (Vdd Vss CLK output0 output1 output2 output3 output4 output5 output6\

output7 output8 output9 output10 output11 output12 output13 output14\

output15 out0 out1 out2 out3 out4 out5 out6 out7 out8 out9\

out10 out11 out12 out13 out14 out15 ) Register16b

AdderSubtractor (Vdd Vss S0 inputAAddSub0 inputAAddSub1 inputAAddSub2 inputAAddSub3\

inputAAddSub4 inputAAddSub5 inputAAddSub6 inputAAddSub7 inputAAddSub8\

inputAAddSub9 inputAAddSub10 inputAAddSub11 inputAAddSub12 inputAAddSub13\

inputAAddSub14 inputAAddSub15 inputBAddSub0 inputBAddSub1 inputBAddSub2\

inputBAddSub3 inputBAddSub4 inputBAddSub5 inputBAddSub6 inputBAddSub7\

inputBAddSub8 inputBAddSub9 inputBAddSub10 inputBAddSub11 inputBAddSub12\

inputBAddSub13 inputBAddSub14 inputBAddSub15 CoutputAdd outputAddSub0\

outputAddSub1 outputAddSub2 outputAddSub3 outputAddSub4 outputAddSub5\

outputAddSub6 outputAddSub7 outputAddSub8 outputAddSub9 outputAddSub10\

outputAddSub11 outputAddSub12 outputAddSub13 outputAddSub14 outputAddSub15\

) SubAdd16b

Shift (Vdd Vss inputASh0 inputASh1 inputASh2 inputASh3 inputASh4 inputASh5 inputASh6 inputASh7 inputASh8 inputASh9\

inputASh10 inputASh11 inputASh12 inputASh13 inputASh14 inputASh15 inputBSh0 inputBSh1 outputSh0 outputSh1\

outputSh2 outputSh3 outputSh4 outputSh5 outputSh6 outputSh7 outputSh8 outputSh9 outputSh10\

outputSh11 outputSh12 outputSh13 outputSh14 outputSh15) Shifter16b

And (Vdd Vss inputAAnd0 inputAAnd1 inputAAnd2 inputAAnd3 inputAAnd4 inputAAnd5 inputAAnd6\

inputAAnd7 inputAAnd8 inputAAnd9 inputAAnd10 inputAAnd11\

inputAAnd12 inputAAnd13 inputAAnd14 inputAAnd15 inputBAnd0 inputBAnd1 inputBAnd2\

inputBAnd3 inputBAnd4 inputBAnd5 inputBAnd6 inputBAnd7 inputBAnd8 inputBAnd9\

inputBAnd10 inputBAnd11 inputBAnd12 inputBAnd13 inputBAnd14 inputBAnd15 outputAnd0\

outputAnd1 outputAnd2 outputAnd3 outputAnd4 outputAnd5\

outputAnd6 outputAnd7 outputAnd8 outputAnd9 outputAnd10 outputAnd11\

outputAnd12 outputAnd13 outputAnd14 outputAnd15) AND2in16b

PassA (Vdd Vss inputAP0 inputAP1 inputAP2 inputAP3 inputAP4 inputAP5 inputAP6 inputAP7 inputAP8\

inputAP9 inputAP10 inputAP11 inputAP12 inputAP13 inputAP14 inputAP15 outputP0 outputP1\

outputP2 outputP3 outputP4 outputP5 outputP6 outputP7 outputP8 outputP9 outputP10\

outputP11 outputP12 outputP13 outputP14 outputP15) PassA16

Or (Vdd Vss inputAOr0 inputAOr1 inputAOr2 inputAOr3 inputAOr4 inputAOr5 inputAOr6 inputAOr7 inputAOr8 inputAOr9\

inputAOr10 inputAOr11 inputAOr12 inputAOr13 inputAOr14 inputAOr15 inputBOr0 inputBOr1 inputBOr2 inputBOr3 inputBOr4\

inputBOr5 inputBOr6 inputBOr7 inputBOr8 inputBOr9 inputBOr10 inputBOr11 inputBOr12 inputBOr13 inputBOr14\

inputBOr15 outputOr0 outputOr1 outputOr2 outputOr3 outputOr4 outputOr5 outputOr6 outputOr7 outputOr8 outputOr9 outputOr10\

outputOr11 outputOr12 outputOr13 outputOr14 outputOr15) OR2in16b

Multiplier (Vdd Vss inputAMult0 inputAMult1 inputAMult2 inputAMult3 inputAMult4 inputAMult5 inputAMult6 inputAMult7\

inputBMult0 inputBMult1 inputBMult2

inputBMult3 inputBMult4 inputBMult5 inputBMult6 inputBMult7 outputMult0\

outputMult1 outputMult2 outputMult3 outputMult4 outputMult5 outputMult6 outputMult7 outputMult8 outputMult9 outputMult10 outputMult11 \

outputMult12 outputMult13 outputMult14 outputMult15) Mult

FinalMux (output0 output1 output2 output3 output4 output5 output6 output7 output8\

output9 output10 output11 output12 output13 output14 output15 outputP0\

outputP1 outputP2 outputP3 outputP4 outputP5 outputP6 outputP7 outputP8 outputP9\

outputP10 outputP11 outputP12 outputP13 outputP14 outputP15 outputAddSub0\

outputAddSub1 outputAddSub2 outputAddSub3 outputAddSub4 outputAddSub5\

outputAddSub6 outputAddSub7 outputAddSub8 outputAddSub9 outputAddSub10\

outputAddSub11 outputAddSub12 outputAddSub13 outputAddSub14 outputAddSub15\

outputAddSub0 outputAddSub1 outputAddSub2 outputAddSub3 outputAddSub4 \

outputAddSub5 outputAddSub6 outputAddSub7 outputAddSub8 outputAddSub9\

outputAddSub10 outputAddSub11 outputAddSub12 outputAddSub13 outputAddSub14\

outputAddSub15 outputSh0 outputSh1 outputSh2 outputSh3 outputSh4 outputSh5\

outputSh6 outputSh7 outputSh8 outputSh9 outputSh10 outputSh11 outputSh12\

outputSh13 outputSh14 outputSh15 outputAnd0 outputAnd1 outputAnd2 outputAnd3\

outputAnd4 outputAnd5 outputAnd6 outputAnd7 outputAnd8 outputAnd9\

outputAnd10 outputAnd11 outputAnd12 outputAnd13 outputAnd14 outputAnd15\

outputOr0 outputOr1 outputOr2 outputOr3 outputOr4 outputOr5 outputOr6\

outputOr7 outputOr8 outputOr9 outputOr10 outputOr11 outputOr12 outputOr13\

outputOr14 outputOr15 outputMult0 outputMult1 outputMult2 outputMult3\

outputMult4 outputMult5 outputMult6 outputMult7 outputMult8 outputMult9\

outputMult10 outputMult11 outputMult12 outputMult13 outputMult14\

outputMult15 output0 output1 output2 output3 output4 output5 output6 output7\

output8 output9 output10 output11 output12 output13 output14 output15 S0 S1\

S2 Vdd Vss) MUX16b81

ends ALU

//End of Subcircuit Definitions

//////////////

//TEST BENCH//

////////////////////////////////////////////////////////////////////////////////////

//Input Buffers:

BuffA0 (vdd! 0 inputA0 A0Buff) bcInverter

BuffA0b (vdd! 0 A0Buff inpA0) bcInverter

BuffB0 (vdd! 0 inputB0 B0Buff) bcInverter

BuffB0b (vdd! 0 B0Buff inpB0) bcInverter

BuffA1 (vdd! 0 inputA1 A1Buff) bcInverter

BuffA1b (vdd! 0 A1Buff inpA1) bcInverter

BuffB1 (vdd! 0 inputB1 B1Buff) bcInverter

BuffB1b (vdd! 0 B1Buff inpB1) bcInverter

BuffA2 (vdd! 0 inputA2 A2Buff) bcInverter

BuffA2b (vdd! 0 A2Buff inpA2) bcInverter

BuffB2 (vdd! 0 inputB2 B2Buff) bcInverter

BuffB2b (vdd! 0 B2Buff inpB2) bcInverter

BuffA3 (vdd! 0 inputA3 A3Buff) bcInverter

BuffA3b (vdd! 0 A3Buff inpA3) bcInverter

BuffB3 (vdd! 0 inputB3 B3Buff) bcInverter

BuffB3b (vdd! 0 B3Buff inpB3) bcInverter

BuffA4 (vdd! 0 inputA4 A4Buff) bcInverter

BuffA4b (vdd! 0 A4Buff inpA4) bcInverter

BuffB4 (vdd! 0 inputB4 B4Buff) bcInverter

BuffB4b (vdd! 0 B4Buff inpB4) bcInverter

BuffA5 (vdd! 0 inputA5 A5Buff) bcInverter

BuffA5b (vdd! 0 A5Buff inpA5) bcInverter

BuffB5 (vdd! 0 inputB5 B5Buff) bcInverter

BuffB5b (vdd! 0 B5Buff inpB5) bcInverter

BuffA6 (vdd! 0 inputA6 A6Buff) bcInverter

BuffA6b (vdd! 0 A6Buff inpA6) bcInverter

BuffB6 (vdd! 0 inputB6 B6Buff) bcInverter

BuffB6b (vdd! 0 B6Buff inpB6) bcInverter

BuffA7 (vdd! 0 inputA7 A7Buff) bcInverter

BuffA7b (vdd! 0 A7Buff inpA7) bcInverter

BuffB7 (vdd! 0 inputB7 B7Buff) bcInverter

BuffB7b (vdd! 0 B7Buff inpB7) bcInverter

BuffA8 (vdd! 0 inputA8 A8Buff) bcInverter

BuffA8b (vdd! 0 A8Buff inpA8) bcInverter

BuffB8 (vdd! 0 inputB8 B8Buff) bcInverter

BuffB8b (vdd! 0 B8Buff inpB8) bcInverter

BuffA9 (vdd! 0 inputA9 A9Buff) bcInverter

BuffA9b (vdd! 0 A9Buff inpA9) bcInverter

BuffB9 (vdd! 0 inputB9 B9Buff) bcInverter

BuffB9b (vdd! 0 B9Buff inpB9) bcInverter

BuffA10 (vdd! 0 inputA10 A10Buff) bcInverter

BuffA10b (vdd! 0 A10Buff inpA10) bcInverter

BuffB10 (vdd! 0 inputB10 B10Buff) bcInverter

BuffB10b (vdd! 0 B10Buff inpB10) bcInverter

BuffA11 (vdd! 0 inputA11 A11Buff) bcInverter

BuffA11b (vdd! 0 A11Buff inpA11) bcInverter

BuffB11 (vdd! 0 inputB11 B11Buff) bcInverter

BuffB11b (vdd! 0 B11Buff inpB11) bcInverter

BuffA12 (vdd! 0 inputA12 A12Buff) bcInverter

BuffA12b (vdd! 0 A12Buff inpA12) bcInverter

BuffB12 (vdd! 0 inputB12 B120Buff) bcInverter

BuffB12b (vdd! 0 B120Buff inpB12) bcInverter

BuffA13 (vdd! 0 inputA13 A13Buff) bcInverter

BuffA13b (vdd! 0 A13Buff inpA13) bcInverter

BuffB13 (vdd! 0 inputB13 B13Buff) bcInverter

BuffB13b (vdd! 0 B13Buff inpB13) bcInverter

BuffA14 (vdd! 0 inputA14 A14Buff) bcInverter

BuffA14b (vdd! 0 A14Buff inpA14) bcInverter

BuffB14 (vdd! 0 inputB14 B14Buff) bcInverter

BuffB14b (vdd! 0 B14Buff inpB14) bcInverter

BuffA15 (vdd! 0 inputA15 A15Buff) bcInverter

BuffA15b (vdd! 0 A15Buff inpA15) bcInverter

BuffB15 (vdd! 0 inputB15 B15Buff) bcInverter

BuffB15b (vdd! 0 B15Buff inpB15) bcInverter

BuffCLK (vdd! 0 CLKIn CBuff) bcInverter

BuffCLKa (vdd! 0 CBuff CLKm) bcInverter

mult=4

BuffCLKb (vdd! 0 CLKm CBuff2) bcInverter mult=16

BuffCLKc (vdd! 0 CBuff2 CLKinput) bcInverter

mult=64

BuffS0 (vdd! 0 S0input S0Buff) bcInverter mult=1

BuffS0b (vdd! 0 S0Buff inpS01) bcInverter

mult=4

BuffS0c (vdd! 0 inpS01 S0Buff1) bcInverter

mult=16

BuffS0d (vdd! 0 S0Buff1 inpS0) bcInverter

mult=64

BuffS1 (vdd! 0 S1input S1Buff) bcInverter mult=1

BuffS1b (vdd! 0 S1Buff inpS11) bcInverter

mult=4

BuffS1c (vdd! 0 inpS11 S1Buff1) bcInverter

mult=16

BuffS1d(vdd! 0 S1Buff1 inpS1) bcInverter

mult=64

BuffS2 (vdd! 0 S2input S2Buff) bcInverter mult=1

BuffS2b (vdd! 0 S2Buff inpS21) bcInverter

mult=4

BuffS2c (vdd! 0 inpS21 S2Buff1) bcInverter

mult=16

BuffS2d (vdd! 0 S2Buff1 inpS2) bcInverter

mult=64

//Input Sources:

// Change these sources depending on test

// If using a pulse, comment out the dc and vice versa

//V0 ( inputA0 0 ) vsource type=dc dc=pvdd

V0p ( inputA0 0 ) vsource type=pulse val0=0 val1=pvdd delay=100n rise=0.01n fall=0.01n width=100n period=200n

V1 ( inputB0 0 ) vsource type=dc dc=pvdd

//V1p ( inputB0 0 ) vsource type=pulse val0=0 val1=pvdd delay=1n rise=0.01n fall=0.01n width=100n period=200n

//V2 ( inputA1 0 ) vsource type=dc dc=pvdd

V2p ( inputA1 0 ) vsource type=pulse val0=pvdd val1=0 delay=100n rise=0.01n fall=0.01n width=100n period=200n

V3 ( inputB1 0 ) vsource type=dc dc=0

//V3p ( inputB1 0 ) vsource type=pulse val0=pvdd val1=0 delay=0n rise=0.01n fall=0.01n width=10n period=20n

//V4 ( inputA2 0 ) vsource type=dc dc=pvdd

V4p ( inputA2 0 ) vsource type=pulse val0=0 val1=pvdd delay=100n rise=0.01n fall=0.01n width=100n period=200n

V5 ( inputB2 0 ) vsource type=dc dc=pvdd

//V5p ( inputB2 0 ) vsource type=pulse val0=0 val1=pvdd delay=1n rise=0.01n fall=0.01n width=400n period=800n

//V6 ( inputA3 0 ) vsource type=dc dc=pvdd

V6p ( inputA3 0 ) vsource type=pulse val0=pvdd val1=0 delay=100n rise=0.01n fall=0.01n width=100n period=200n

V7 ( inputB3 0 ) vsource type=dc dc=0

//V6p ( inputB3 0 ) vsource type=pulse val0=0 val1=pvdd delay=800n rise=0.01n fall=0.01n width=800n period=1600n

//V8 ( inputA4 0 ) vsource type=dc dc=pvdd

V8p ( inputA4 0 ) vsource type=pulse val0=0 val1=pvdd delay=100n rise=0.01n fall=0.01n width=100n period=200n

V9 ( inputB4 0 ) vsource type=dc dc=pvdd

//V9p ( inputB4 0 ) vsource type=pulse val0=0 val1=pvdd delay=1600n rise=0.01n fall=0.01n width=1600n period=3200n

//V10 ( inputA5 0 ) vsource type=dc dc=pvdd

V10p ( inputA5 0 ) vsource type=pulse val0=pvdd val1=0 delay=100n rise=0.01n fall=0.01n width=100n period=200n

V11 ( inputB5 0 ) vsource type=dc dc=0

//V11p ( inputB5 0 ) vsource type=pulse val0=0 val1=pvdd delay=2n rise=0.01n fall=0.01n width=5n period=10n

//V12 ( inputA6 0 ) vsource type=dc dc=pvdd

V12p ( inputA6 0 ) vsource type=pulse val0=0 val1=pvdd delay=100n rise=0.01n fall=0.01n width=100n period=200n

V13 ( inputB6 0 ) vsource type=dc dc=pvdd

//V13p ( inputB6 0 ) vsource type=pulse val0=0 val1=pvdd delay=2n rise=0.01n fall=0.01n width=5n period=10n

//V14 ( inputA7 0 ) vsource type=dc dc=pvdd

V14p ( inputA7 0 ) vsource type=pulse val0=pvdd val1=0 delay=100n rise=0.01n fall=0.01n width=100n period=200n

V15 ( inputB7 0 ) vsource type=dc dc=0

//Vp ( inputB7 0 ) vsource type=pulse val0=0 val1=pvdd delay=2n rise=0.01n fall=0.01n width=5n period=10n

//V16 ( inputA8 0 ) vsource type=dc dc=0

V16p ( inputA8 0 ) vsource type=pulse val0=0 val1=pvdd delay=100n rise=0.01n fall=0.01n width=100n period=200n

V17 ( inputB8 0 ) vsource type=dc dc=0

//V17p ( inputB8 0 ) vsource type=pulse val0=0 val1=pvdd delay=2n rise=0.01n fall=0.01n width=5n period=10n

//V18 ( inputA9 0 ) vsource type=dc dc=0

V18p ( inputA9 0 ) vsource type=pulse val0=pvdd val1=0 delay=100n rise=0.01n fall=0.01n width=100n period=200n

V19 ( inputB9 0 ) vsource type=dc dc=pvdd

//V19p ( inputB9 0 ) vsource type=pulse val0=0 val1=pvdd delay=2n rise=0.01n fall=0.01n width=5n period=10n

//V20 ( inputA10 0 ) vsource type=dc dc=0

V20p ( inputA10 0 ) vsource type=pulse val0=0 val1=pvdd delay=100n rise=0.01n fall=0.01n width=100n period=200n

V21 ( inputB10 0 ) vsource type=dc dc=0

//V21p ( inputB10 0 ) vsource type=pulse val0=0 val1=pvdd delay=2n rise=0.01n fall=0.01n width=5n period=10n

//V22 ( inputA11 0 ) vsource type=dc dc=0

V22p ( inputA11 0 ) vsource type=pulse val0=pvdd val1=0 delay=100n rise=0.01n fall=0.01n width=100n period=200n

V23 ( inputB11 0 ) vsource type=dc dc=pvdd

//V23p ( inputB11 0 ) vsource type=pulse val0=0 val1=pvdd delay=2n rise=0.01n fall=0.01n width=5n period=10n

//V24 ( inputA12 0 ) vsource type=dc dc=0

V24p ( inputA12 0 ) vsource type=pulse val0=0 val1=pvdd delay=100n rise=0.01n fall=0.01n width=100n period=200n

V25 ( inputB12 0 ) vsource type=dc dc=0

//V25p ( inputB12 0 ) vsource type=pulse val0=0 val1=pvdd delay=2n rise=0.01n fall=0.01n width=5n period=10n

//V26 ( inputA13 0 ) vsource type=dc dc=0

V26p ( inputA13 0 ) vsource type=pulse val0=pvdd val1=0 delay=100n rise=0.01n fall=0.01n width=100n period=200n

V27 ( inputB13 0 ) vsource type=dc dc=pvdd

//V27p ( inputB13 0 ) vsource type=pulse val0=0 val1=pvdd delay=2n rise=0.01n fall=0.01n width=5n period=10n

//V28 ( inputA14 0 ) vsource type=dc dc=0

V28p ( inputA14 0 ) vsource type=pulse val0=0 val1=pvdd delay=100n rise=0.01n fall=0.01n width=100n period=200n

V29 ( inputB14 0 ) vsource type=dc dc=0

//V29p ( inputB14 0 ) vsource type=pulse val0=0 val1=pvdd delay=2n rise=0.01n fall=0.01n width=5n period=10n

//V30 ( inputA15 0 ) vsource type=dc dc=0

V30p ( inputA15 0 ) vsource type=pulse val0=pvdd val1=0 delay=100n rise=0.01n fall=0.01n width=100n period=200n

V31 ( inputB15 0 ) vsource type=dc dc=pvdd

//V31p ( inputB15 0 ) vsource type=pulse val0=0 val1=pvdd delay=20n rise=0.01n fall=0.01n width=10n period=40n

V34 ( S0input 0 ) vsource type=dc dc=pvdd

//V34p ( S0input 0 ) vsource type=pulse val0=0 val1=pvdd delay=5n rise=0.01n fall=0.01n width=5n period=10n

RegS0 (CLKinput S0in S0input vdd! 0) Reg1b

V35 ( S1in 0 ) vsource type=dc dc=pvdd

//V35p ( S1in 0 ) vsource type=pulse val0=0 val1=pvdd delay=5n rise=0.01n fall=0.01n width=5n period=10n

RegS1 (CLKinput S1in S1input vdd! 0) Reg1b

V36 ( S2in 0 ) vsource type=dc dc=pvdd

//V36p ( S2in 0 ) vsource type=pulse val0=0 val1=pvdd delay=5n rise=0.01n fall=0.01n width=5n period=10n

RegS2 (CLKinput S2in S2input vdd! 0) Reg1b

V37 ( CLKIn 0 ) vsource type = pulse val0=0 val1=pvdd delay=25n rise=0.01n fall=0.01n width=50n period=100n

//Loads (FO4 inverters)

I19 (vdd! 0 out0 outputS0) bcInverter mult=4

I20 (vdd! 0 out1 outputS1) bcInverter mult=4

I21 (vdd! 0 out2 outputS2) bcInverter mult=4

I22 (vdd! 0 out3 outputS3) bcInverter mult=4

I23 (vdd! 0 out4 outputS4) bcInverter mult=4

I24 (vdd! 0 out5 outputS5) bcInverter mult=4

I25 (vdd! 0 out6 outputS6) bcInverter mult=4

I26 (vdd! 0 out7 outputS7) bcInverter mult=4

I27 (vdd! 0 out8 outputS8) bcInverter mult=4

I28 (vdd! 0 out9 outputS9) bcInverter mult=4

I29 (vdd! 0 out10 outputS10) bcInverter mult=4

I30 (vdd! 0 out11 outputS11) bcInverter mult=4

I31 (vdd! 0 out12 outputS12) bcInverter mult=4

I32 (vdd! 0 out13 outputS13) bcInverter mult=4

I33 (vdd! 0 out14 outputS14) bcInverter mult=4

I34 (vdd! 0 out15 outputS15) bcInverter mult=4

I35 (vdd! 0 Cout Coutput) bcInverter mult=4

//Subcircuit Testing:

// Only un-comment the circuit you are testing!!!

//independent source to measure power:

VALU ( vddALU 0 ) vsource type=dc dc=pvdd

//SubAddTest (vddALU 0 inpS0 inpA0 inpA1 inpA2 inpA3 inpA4 inpA5 inpA6 inpA7 inpA8 inpA9\

// inpA10 inpA11 inpA12 inpA13 inpA14 inpA15 inpB0 inpB1 inpB2 inpB3 inpB4 inpB5 inpB6 inpB7\

// inpB8 inpB9 inpB10 inpB11 inpB12 inpB13 inpB14 inpB15 Cout out0 out1 out2 out3 out4 out5 out6\

// out7 out8 out9 out10 out11 out12 out13 out14 out15) SubAdd16b

//ShiftTest (vddSh 0 inpA0 inpA1 inpA2 inpA3 inpA4 inpA5 inpA6 inpA7 inpA8 inpA9\

// inpA10 inpA11 inpA12 inpA13 inpA14 inpA15 inpB0 inpB1 out0 out1\

// out2 out3 out4 out5 out6 out7 out8 out9 out10\

// out11 out12 out13 out14 out15) Shifter16b

//RegTest (vdd! 0 Cin inpA0 inpA1 inpA2 inpA3 inpA4 inpA5 inpA6 inpA7 inpA8 inpA9\

// inpA10 inpA11 inpA12 inpA13 inpA14 inpA15 out0 out1\

// out2 out3 out4 out5 out6 out7 out8 out9 out10\

// out11 out12 out13 out14 out15) Register16b

//AndTest (vdd! 0 out0 out1 out2 out3 out4 out5 out6 out7 out8 out9 out10 out11 \

// out12 out13 out14 out15 inpA0 inpA1 inpA2 inpA3 inpA4 inpA5 inpA6 inpA7\

// inpA8 inpA9 inpA10 inpA11 inpA12 inpA13 inpA14 inpA15 inpB0 inpB1 inpB2\

// inpB3 inpB4 inpB5 inpB6 inpB7 inpB8 inpB9 inpB10 inpB11 inpB12 inpB13\

// inpB14 inpB15) AND2in16b

//PassATest (vdd! 0 inpA0 inpA1 inpA2 inpA3 inpA4 inpA5 inpA inpA7 inpA8 inpA9 inpA10\

// inpA11 inpA12 inpA13 inpA14 inpA15 out0 out1 out2 out3 out4 out5 out6 out7 \

// out8 out9 out10 out11 out12 out13 out14 out15)

PassA16

ALUTest (vddALU 0 CLKinput inpA0 inpA1 inpA2 inpA3 inpA4 inpA5 inpA6 inpA7 inpA8 inpA9\

inpA10 inpA11 inpA12 inpA13 inpA14 inpA15 inpB0 inpB1 inpB2 inpB3 inpB4 inpB5 inpB6 inpB7\

inpB8 inpB9 inpB10 inpB11 inpB12 inpB13 inpB14 inpB15 inpS0 inpS1 inpS2\

out0 out1 out2 out3 out4 out5 out6 out7 out8 out9 out10 out11 \

out12 out13 out14 out15 Cout) ALU

//multTest (vdd! 0 inpA0 inpA1 inpA2 inpA3 inpA4 inpA5 inpA6 inpA7\

// inpB0 inpB1 inpB2

inpB3 inpB4 inpB5 inpB6 inpB7 out0\

// out1 out2 out3 out4 out5 out6 out7 out8 out9 out10 out11 \

// out12 out13 out14 out15) Mult

//Thank you for reading team NOR's netlist, come again soon!